# QHRAE

# Superior 10AS/10ASG

# LA-7213P REV 1.0 Schematic

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**AMD Llano FS1 Processor / Hudson M2/M3**
**Whistler Pro**

**2011-04-30 Rev 1.0**

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/01/06 | Deciphered Date | 2012/01/06 |

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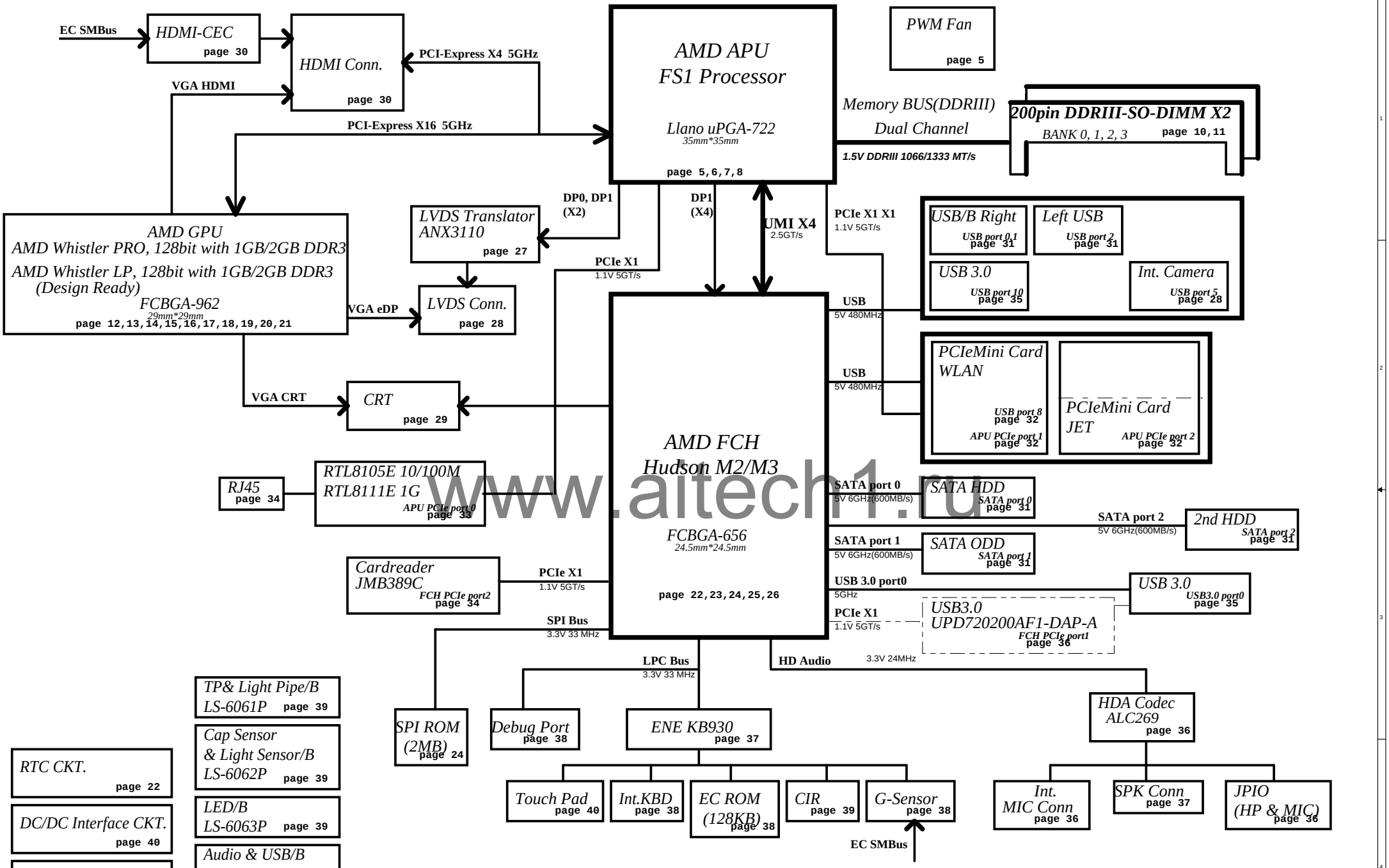
| Size: B | Document Number: 4019D8 | Rev: B |
| Date: Monday, July 04, 2011 | Sheet 1 of 51 | |

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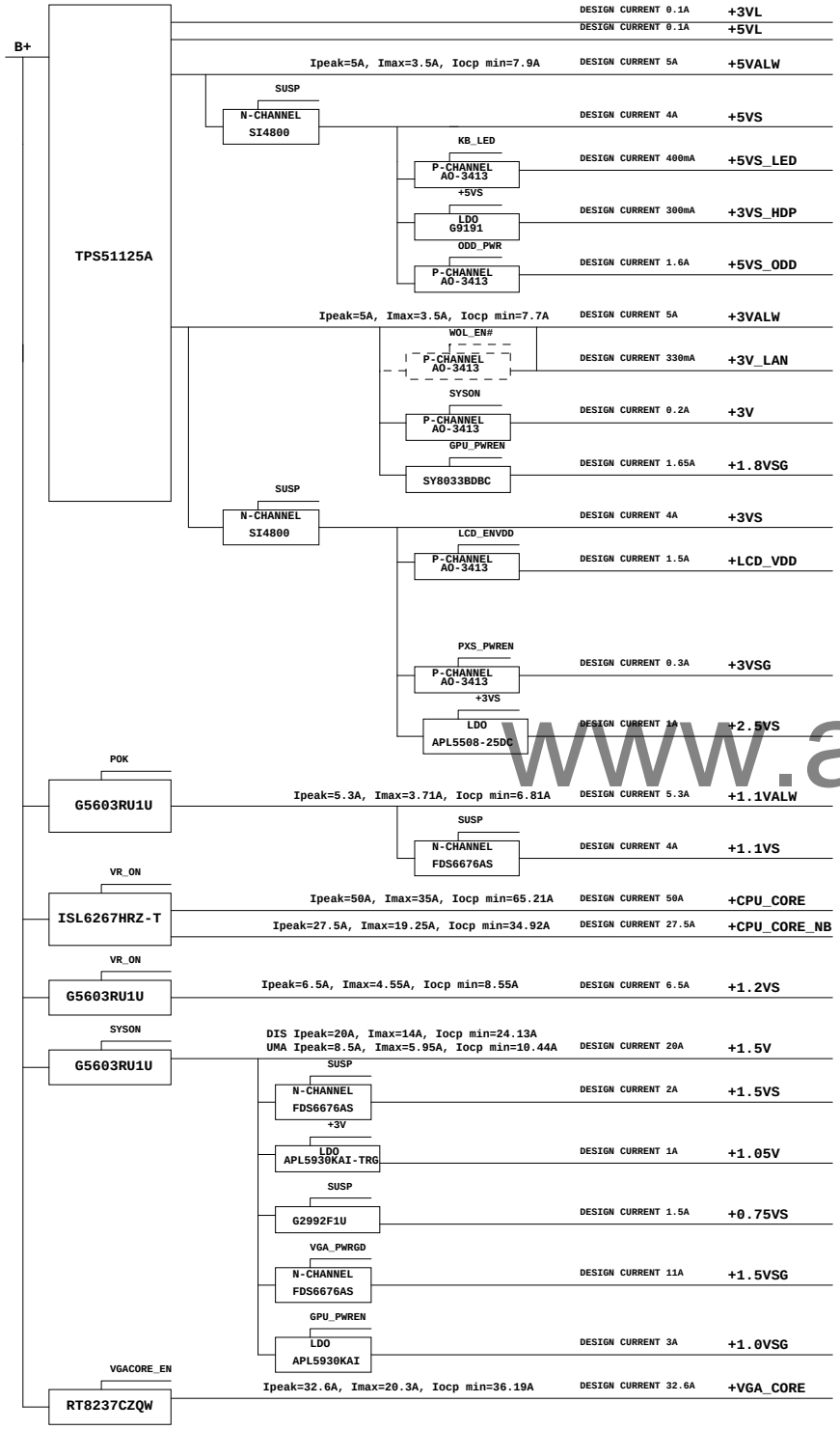


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## Voltage Rails

( O MEANS ON X MEANS OFF )

| power plane / State | +RTCVCC | B+ | +5VL<br>+3VL | +5VALW<br>+3VALW<br>+1.1VALW<br>+VSB | +1.5V<br>+3V<br>+1.05V | +5VS<br>+3VS<br>+2.5VS<br>+1.5VS<br>+1.2VS<br>+1.1VS<br>+0.75VS<br>+CPU_CORE<br>+CPU_CORE_NB<br>+VGA_CORE<br>+3VSG<br>+1.8VSG<br>+1.5VSG<br>+1.0VSG |
|---|---|---|---|---|---|---|
| S0 | 0 | 0 | 0 | 0 | 0 | 0 |
| S1 | 0 | 0 | 0 | 0 | 0 | 0 |
| S3 | 0 | 0 | 0 | 0 | 0 | X |
| S5 S4/AC | 0 | 0 | 0 | 0 | X | X |
| S5 S4/ Battery only | 0 | 0 | 0 | X | X | X |
| S5 S4/AC & Battery don't exist | 0 | X | X | X | X | X |

## BTO Option Table

| Function | HDMI | | | | SKU | | |
|---|---|---|---|---|---|---|---|
| description | HDMI | | | | SKU | | |
| explain | UMA PowerXpress | Discrete | COMMON | CEC | UMA | PowerXpress | Discrete |
| BTO | IHDMI@ | DHDMI@ | HDMI@ | CEC@ | UMA@ | UMA@+VGA@+PXS@ | VGA@+DIS@ |

| Function | | LAN | | CIR | KB Light |
|---|---|---|---|---|---|
| description | | LAN | | CIR | KB Light |
| explain | | 10/100M | GIGA | CIR | KB Light |
| BTO | | 8105E@ | 8111E@ | CIR@ | KBL@ |

| Function | | G-SENSOR | Cam & Mic | Panel | | |
|---|---|---|---|---|---|---|
| description | | G-SENSOR | Cam & Mic | Panel (DIS@) | | |
| explain | | G-SENSOR | Cam & Mic | 3D LVDS | eDP | Non-3D & EDP |
| BTO | | GSENSOR@ | CAM@ | 3D@+NOEDP@ | EDP@ | NO3D@+NOEDP@ |

| Function | GPIO for PowerXpress | | Chipset | | | |
|---|---|---|---|---|---|---|
| description | PowerXpress (PXS@) | | FCH | | GPU | |
| explain | PowerXpress Enable | Crossfire Enable | Hudson-M3 | | Whistler Pro | |
| BTO | PXSEN@ | CROSSEN@ | HUDM3R1@ | HUDM3R3@ | WHPROR1@ | WHPROR3@ |

| Function | PowerXpress | | Renesas USB3.0 | FCH | | EC | |
|---|---|---|---|---|---|---|---|
| description | PowerXpress (PXS@) | | Renesas USB3.0 | FCH | | EC | |
| explain | BACO mode | Non-BACO | Renesas USB3.0 | Hudson-M2 | Hudson-M3 | KB-930 | KB-9012 |
| BTO | BACO@ | NOBACO@ | RENE@ | M2@ | M3@ | KB930@ | KB9012@ |

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## FCH SM Bus Address (SCL0/SDA0)

| Power | Device | HEX | Address |
|---|---|---|---|
| +3VS | DDR SO-DIMM 0 | A0 H | 1010 0000 b |
| +3VS | DDR SO-DIMM 1 | A4 H | 1010 0100 b |
| +3VS | WLAN | | |
| +3VS | 3G | | |

## EC SM Bus1 Address

| Power | Device | HEX | Address |
|---|---|---|---|
| +3VL | Smart Battery | 16 H | 0001 0110 b |
| +3VL | HDMI-CEC | 34 H | 0011 0100 b |

| Power | Device | HEX | Address |
|---|---|---|---|
| +3VL | Cap. Sensor | | Virtual I2C |

## EC SM Bus2 Address

| Power | Device | HEX | Address |
|---|---|---|---|
| +3VS | CPU Thermal Sensor | 98 H | 1001 1001 b |
| +3VS | GPU Thermal Sensor | 41 H | 0100 0001 b |
| +3VS | G-Sensor | 40 H | 0100 0000 b |
| +3VS | Light Sensor | 52 H | 0101 0010 b |
| +3VS | 3D - Bootloader | C0 H | 1100 0000 b |
| +3VS | 3D - Slave | C0 H | 1100 0000 b |

| STATE / SIGNAL | SLP_S3# | SLP_S5# |
|---|---|---|
| Full ON | HIGH | HIGH |
| S1(Power On Suspend) | HIGH | HIGH |
| S3 (Suspend to RAM) | LOW | HIGH |
| S4 (Suspend to Disk) | LOW | HIGH |
| S5 (Soft OFF) | LOW | LOW |
| G3 | LOW | LOW |

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12 PCIE_GTX_C_FRX_P[0..15]
12 PCIE_GTX_C_FRX_N[0..15]

PCIE_FTX_C_GRX_P[0..15] 12
PCIE_FTX_C_GRX_N[0..15] 12

JAPUA @

PCI EXPRESS

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| PCIE_GTX_C_FRX_P0 | AA8 | P_GFX_RXP0 | P_GFX_TXP0 | AA2 | PCIE_FTX_GRX_P0 | C1 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P0 |
| PCIE_GTX_C_FRX_N0 | AA9 | P_GFX_RXN0 | P_GFX_TXN0 | AA3 | PCIE_FTX_GRX_N0 | C2 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N0 |
| PCIE_GTX_C_FRX_P1 | Y7 | P_GFX_RXP1 | P_GFX_TXP1 | Y2 | PCIE_FTX_GRX_P1 | C3 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P1 |
| PCIE_GTX_C_FRX_N1 | Y8 | P_GFX_RXN1 | P_GFX_TXN1 | Y1 | PCIE_FTX_GRX_N1 | C4 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N1 |
| PCIE_GTX_C_FRX_P2 | W5 | P_GFX_RXP2 | P_GFX_TXP2 | Y4 | PCIE_FTX_GRX_P2 | C9 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P2 |
| PCIE_GTX_C_FRX_N2 | W6 | P_GFX_RXN2 | P_GFX_TXN2 | Y5 | PCIE_FTX_GRX_N2 | C22 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N2 |
| PCIE_GTX_C_FRX_P3 | W8 | P_GFX_RXP3 | P_GFX_TXP3 | W2 | PCIE_FTX_GRX_P3 | C23 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P3 |
| PCIE_GTX_C_FRX_N3 | W9 | P_GFX_RXN3 | P_GFX_TXN3 | W3 | PCIE_FTX_GRX_N3 | C24 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N3 |
| PCIE_GTX_C_FRX_P4 | V7 | P_GFX_RXP4 | P_GFX_TXP4 | V2 | PCIE_FTX_GRX_P4 | C25 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P4 |
| PCIE_GTX_C_FRX_N4 | V8 | P_GFX_RXN4 | P_GFX_TXN4 | V1 | PCIE_FTX_GRX_N4 | C26 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N4 |
| PCIE_GTX_C_FRX_P5 | U5 | P_GFX_RXP5 | P_GFX_TXP5 | V4 | PCIE_FTX_GRX_P5 | C27 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P5 |
| PCIE_GTX_C_FRX_N5 | U6 | P_GFX_RXN5 | P_GFX_TXN5 | V5 | PCIE_FTX_GRX_N5 | C28 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N5 |
| PCIE_GTX_C_FRX_P6 | U8 | P_GFX_RXP6 | P_GFX_TXP6 | U2 | PCIE_FTX_GRX_P6 | C29 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P6 |
| PCIE_GTX_C_FRX_N6 | U9 | P_GFX_RXN6 | P_GFX_TXN6 | U3 | PCIE_FTX_GRX_N6 | C30 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N6 |
| PCIE_GTX_C_FRX_P7 | T7 | P_GFX_RXP7 | P_GFX_TXP7 | T2 | PCIE_FTX_GRX_P7 | C31 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P7 |
| PCIE_GTX_C_FRX_N7 | T8 | P_GFX_RXN7 | P_GFX_TXN7 | T1 | PCIE_FTX_GRX_N7 | C32 | 1 | 2 | VGA@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N7 |
| PCIE_GTX_C_FRX_P8 | R5 | P_GFX_RXP8 | P_GFX_TXP8 | T4 | PCIE_FTX_GRX_P8 | C33 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P8 |
| PCIE_GTX_C_FRX_N8 | R6 | P_GFX_RXN8 | P_GFX_TXN8 | T5 | PCIE_FTX_GRX_N8 | C34 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N8 |
| PCIE_GTX_C_FRX_P9 | R8 | P_GFX_RXP9 | P_GFX_TXP9 | R2 | PCIE_FTX_GRX_P9 | C35 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P9 |
| PCIE_GTX_C_FRX_N9 | R9 | P_GFX_RXN9 | P_GFX_TXN9 | R3 | PCIE_FTX_GRX_N9 | C36 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N9 |
| PCIE_GTX_C_FRX_P10 | P7 | P_GFX_RXP10 | P_GFX_TXP10 | P2 | PCIE_FTX_GRX_P10 | C37 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P10 |
| PCIE_GTX_C_FRX_N10 | P8 | P_GFX_RXN10 | P_GFX_TXN10 | P1 | PCIE_FTX_GRX_N10 | C38 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N10 |
| PCIE_GTX_C_FRX_P11 | N5 | P_GFX_RXP11 | P_GFX_TXP11 | P4 | PCIE_FTX_GRX_P11 | C39 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P11 |
| PCIE_GTX_C_FRX_N11 | N6 | P_GFX_RXN11 | P_GFX_TXN11 | P5 | PCIE_FTX_GRX_N11 | C40 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N11 |
| PCIE_GTX_C_FRX_P12 | N8 | P_GFX_RXP12 | P_GFX_TXP12 | N2 | PCIE_FTX_GRX_P12 | C41 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P12 |
| PCIE_GTX_C_FRX_N12 | N9 | P_GFX_RXN12 | P_GFX_TXN12 | N3 | PCIE_FTX_GRX_N12 | C42 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N12 |
| PCIE_GTX_C_FRX_P13 | M7 | P_GFX_RXP13 | P_GFX_TXP13 | M2 | PCIE_FTX_GRX_P13 | C43 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P13 |
| PCIE_GTX_C_FRX_N13 | M8 | P_GFX_RXN13 | P_GFX_TXN13 | M1 | PCIE_FTX_GRX_N13 | C44 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N13 |
| PCIE_GTX_C_FRX_P14 | L5 | P_GFX_RXP14 | P_GFX_TXP14 | M4 | PCIE_FTX_GRX_P14 | C45 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P14 |
| PCIE_GTX_C_FRX_N14 | L6 | P_GFX_RXN14 | P_GFX_TXN14 | M5 | PCIE_FTX_GRX_N14 | C46 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N14 |
| PCIE_GTX_C_FRX_P15 | L8 | P_GFX_RXP15 | P_GFX_TXP15 | L2 | PCIE_FTX_GRX_P15 | C47 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_P15 |
| PCIE_GTX_C_FRX_N15 | L9 | P_GFX_RXN15 | P_GFX_TXN15 | L3 | PCIE_FTX_GRX_N15 | C48 | 1 | 2 | DIS@ 0.1U_0402_16V7K | PCIE_FTX_C_GRX_N15 |

GRAPHICS

For PowerXpress

Place R1 ~ R8 close to C33 ~ C40

| | | | | | |
|---|---|---|---|---|---|
| PCIE_FTX_GRX_P8 | R1 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TX2+ | 30 |
| PCIE_FTX_GRX_N8 | R2 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TX2- | 30 |
| PCIE_FTX_GRX_P9 | R3 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TX1+ | 30 |
| PCIE_FTX_GRX_N9 | R4 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TX1- | 30 |
| PCIE_FTX_GRX_P10 | R5 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TX0+ | 30 |
| PCIE_FTX_GRX_N10 | R6 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TX0- | 30 |
| PCIE_FTX_GRX_P11 | R7 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TXC+ | 30 |
| PCIE_FTX_GRX_N11 | R8 | 1 HDMI@ 2 | 0_0402_5% | UMA_HDMI_TXC- | 30 |

GPP

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 33 PCIE_FRX_C_LANTX_P0 | PCIE_FRX_C_LANTX_P0 | AC5 | P_GPP_RXP0 | P_GPP_TXP0 | AD4 | PCIE_FTX_LANRX_P0 | C49 | 1 | 2 | 0.1U_0402_16V7K | PCIE_FTX_C_LANRX_P0 33 |
| 33 PCIE_FRX_C_LANTX_N0 | PCIE_FRX_C_LANTX_N0 | AC6 | P_GPP_RXN0 | P_GPP_TXN0 | AD5 | PCIE_FTX_LANRX_N0 | C50 | 1 | 2 | 0.1U_0402_16V7K | PCIE_FTX_C_LANRX_N0 33 |
| 32 PCIE_FRX_WLANTX_P1 | PCIE_FRX_WLANTX_P1 | AC8 | P_GPP_RXP1 | P_GPP_TXP1 | AC2 | PCIE_FTX_WLANRX_P1 | C51 | 1 | 2 | 0.1U_0402_16V7K | PCIE_FTX_C_WLANRX_P1 32 |
| 32 PCIE_FRX_WLANTX_N1 | PCIE_FRX_WLANTX_N1 | AC9 | P_GPP_RXN1 | P_GPP_TXN1 | AC3 | PCIE_FTX_WLANRX_N1 | C52 | 1 | 2 | 0.1U_0402_16V7K | PCIE_FTX_C_WLANRX_N1 32 |
| 32 PCIE_FRX_JETTX_P2 | PCIE_FRX_JETTX_P2 | AB7 | P_GPP_RXP2 | P_GPP_TXP2 | AB2 | PCIE_FTX_JETRX_P2 | C53 | 1 | 2 | 0.1U_0402_16V7K | PCIE_FTX_C_JETRX_P2 32 |
| 32 PCIE_FRX_JETTX_N2 | PCIE_FRX_JETTX_N2 | AB8 | P_GPP_RXN2 | P_GPP_TXN2 | AB1 | PCIE_FTX_JETRX_N2 | C54 | 1 | 2 | 0.1U_0402_16V7K | PCIE_FTX_C_JETRX_N2 32 |
| | | AA5 | P_GPP_RXP3 | P_GPP_TXP3 | AB4 | | | | | | |
| | | AA6 | P_GPP_RXN3 | P_GPP_TXN3 | AB5 | | | | | | |

LAN

WLAN

JET

UMI-LINK

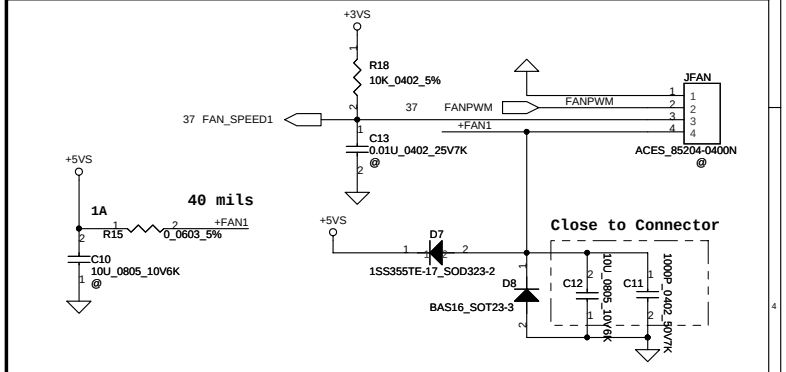
| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 22 UMI_MTX_C_FRX_P0 | UMI_MTX_C_FRX_P0 | AF8 | P_UMI_RXP0 | P_UMI_TXP0 | AF1 | UMI_FTX_MRX_P0 | C55 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_P0 22 |
| 22 UMI_MTX_C_FRX_N0 | UMI_MTX_C_FRX_N0 | AF7 | P_UMI_RXN0 | P_UMI_TXN0 | AF2 | UMI_FTX_MRX_N0 | C56 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_N0 22 |
| 22 UMI_MTX_C_FRX_P1 | UMI_MTX_C_FRX_P1 | AF6 | P_UMI_RXP1 | P_UMI_TXP1 | AF5 | UMI_FTX_MRX_P1 | C57 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_P1 22 |
| 22 UMI_MTX_C_FRX_N1 | UMI_MTX_C_FRX_N1 | AF5 | P_UMI_RXN1 | P_UMI_TXN1 | AF4 | UMI_FTX_MRX_N1 | C58 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_N1 22 |
| 22 UMI_MTX_C_FRX_P2 | UMI_MTX_C_FRX_P2 | AF9 | P_UMI_RXP2 | P_UMI_TXP2 | AF3 | UMI_FTX_MRX_P2 | C59 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_P2 22 |
| 22 UMI_MTX_C_FRX_N2 | UMI_MTX_C_FRX_N2 | AF8 | P_UMI_RXN2 | P_UMI_TXN2 | AF2 | UMI_FTX_MRX_N2 | C60 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_N2 22 |
| 22 UMI_MTX_C_FRX_P3 | UMI_MTX_C_FRX_P3 | AD8 | P_UMI_RXP3 | P_UMI_TXP3 | AD1 | UMI_FTX_MRX_P3 | C61 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_P3 22 |
| 22 UMI_MTX_C_FRX_N3 | UMI_MTX_C_FRX_N3 | AD7 | P_UMI_RXN3 | P_UMI_TXN3 | AD2 | UMI_FTX_MRX_N3 | C62 | 1 | 2 | 0.1U_0402_16V7K | UMI_FTX_C_MRX_N3 22 |

+1.2VS — R9 196_0402_1% — P_ZVDDP K5 — P_ZVDDP

P_ZVSS K4 — R10 196_0402_1%

AMD_TOPEDO_FS-1

## FAN Control Circuit

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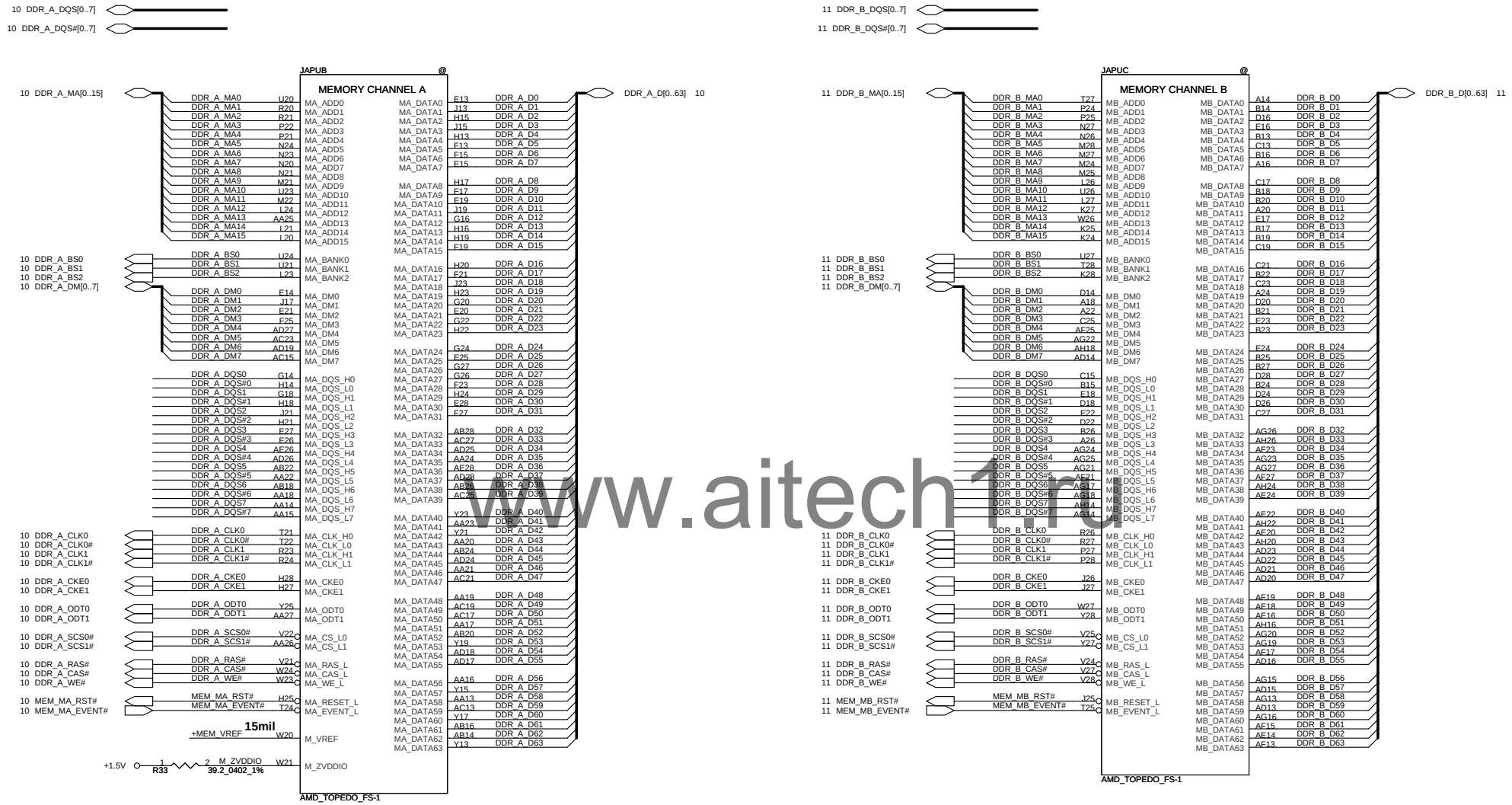


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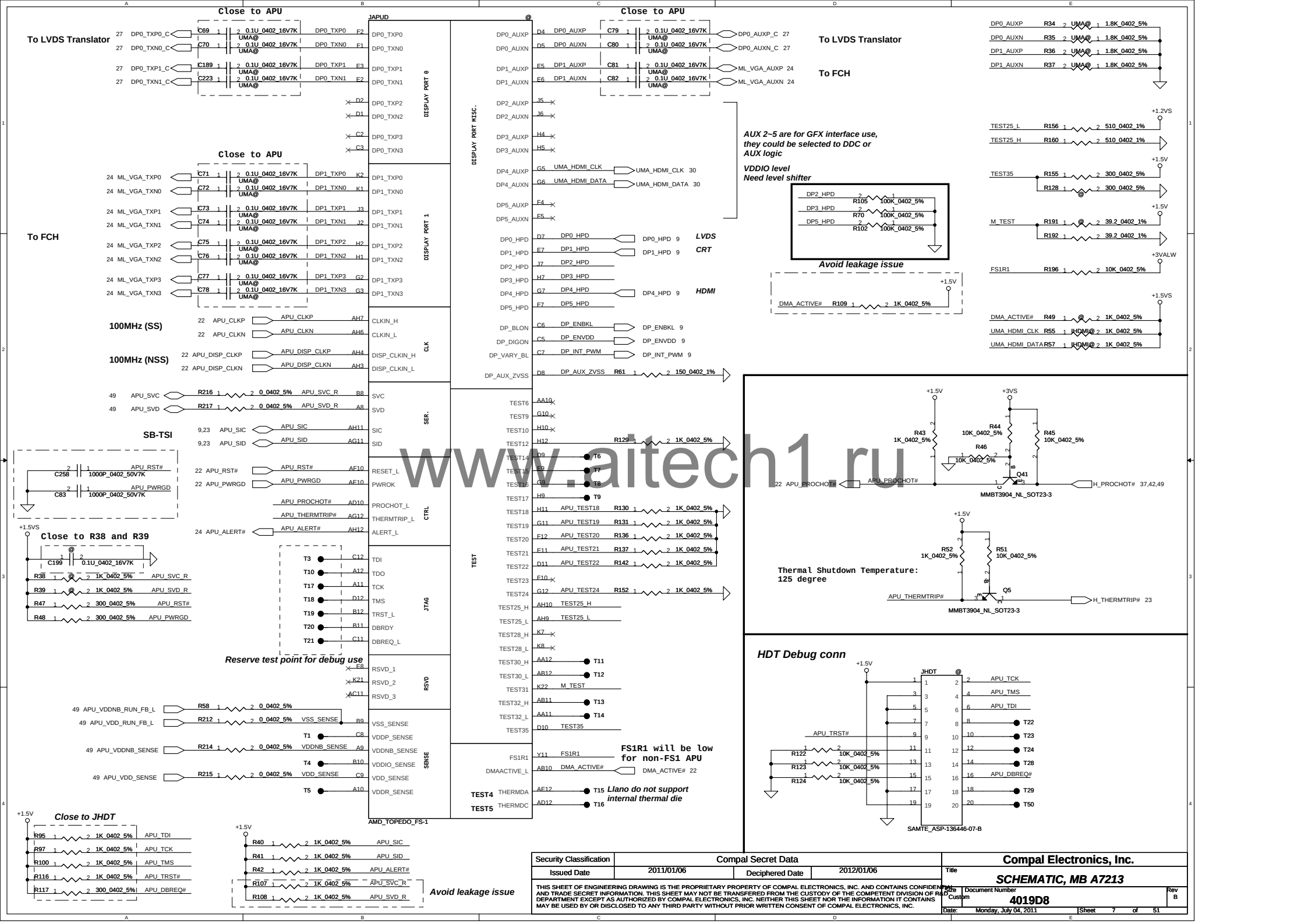


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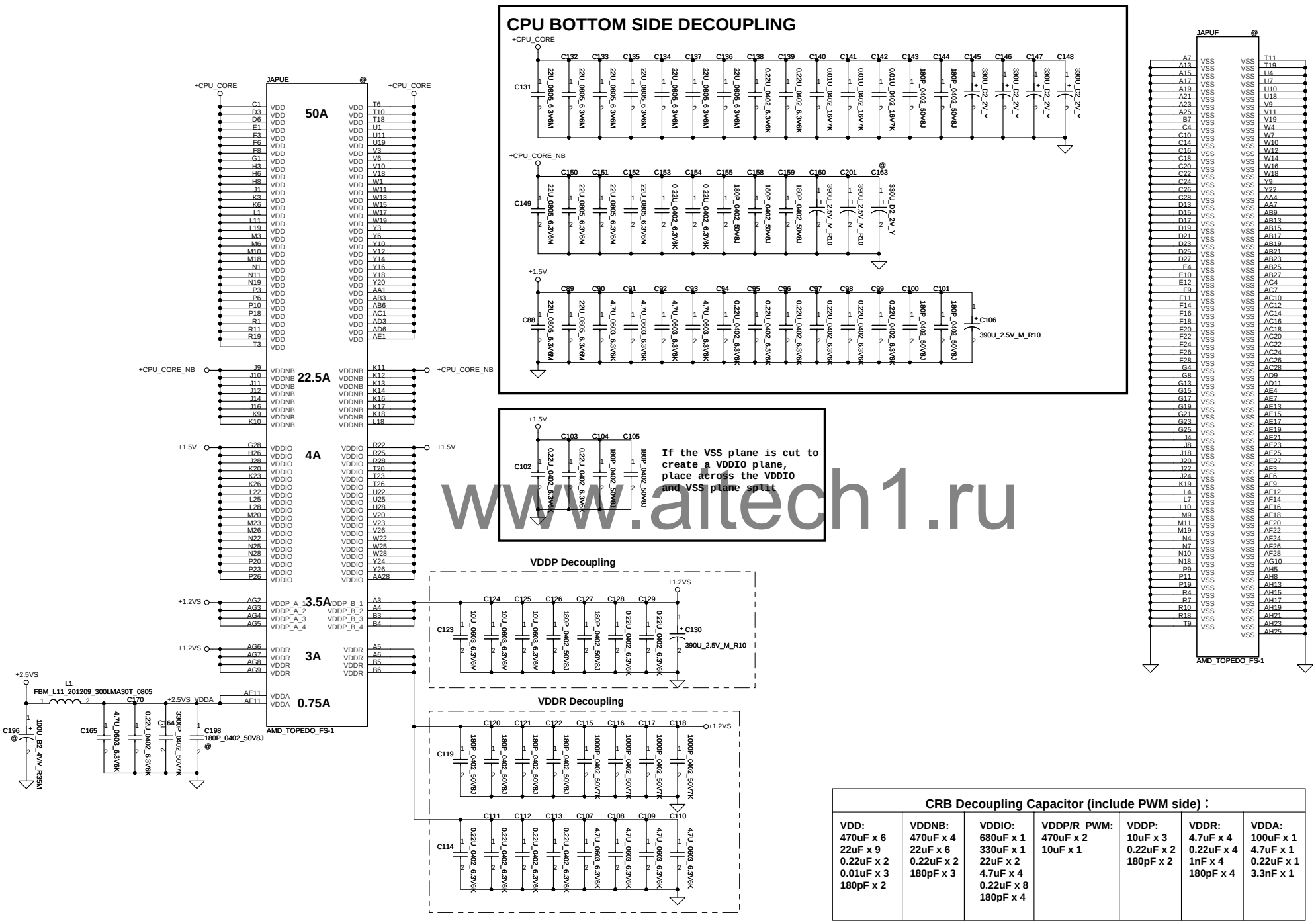


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## CRB Decoupling Capacitor (include PWM side) :

| VDD: | VDDNB: | VDDIO: | VDDP/R_PWM: | VDDP: | VDDR: | VDDA: |
|---|---|---|---|---|---|---|
| 470uF x 6<br>22uF x 9<br>0.22uF x 2<br>0.01uF x 3<br>180pF x 2 | 470uF x 4<br>22uF x 6<br>0.22uF x 2<br>180pF x 3 | 680uF x 1<br>330uF x 1<br>22uF x 2<br>4.7uF x 4<br>0.22uF x 8<br>180pF x 4 | 470uF x 2<br>10uF x 1 | 10uF x 3<br>0.22uF x 2<br>180pF x 2 | 4.7uF x 4<br>0.22uF x 4<br>1nF x 4<br>180pF x 4 | 100uF x 1<br>4.7uF x 1<br>0.22uF x 1<br>3.3nF x 1 |

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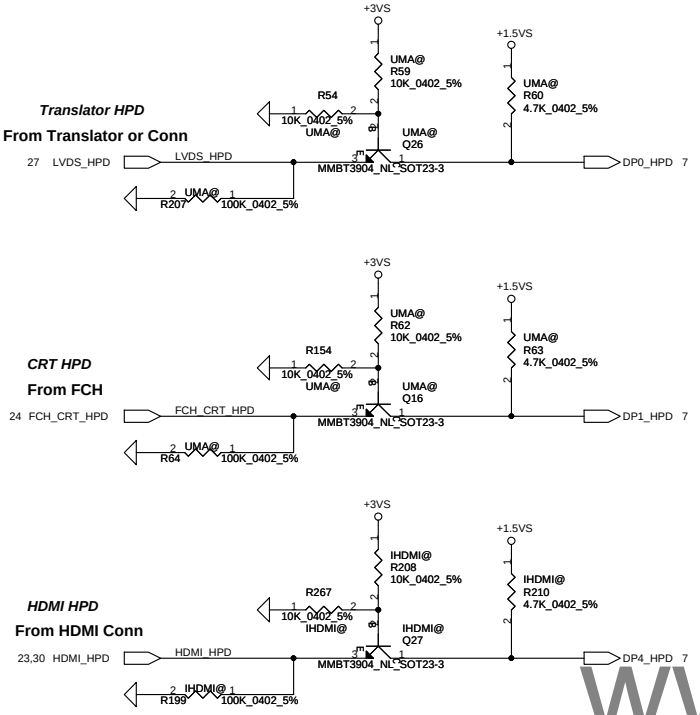
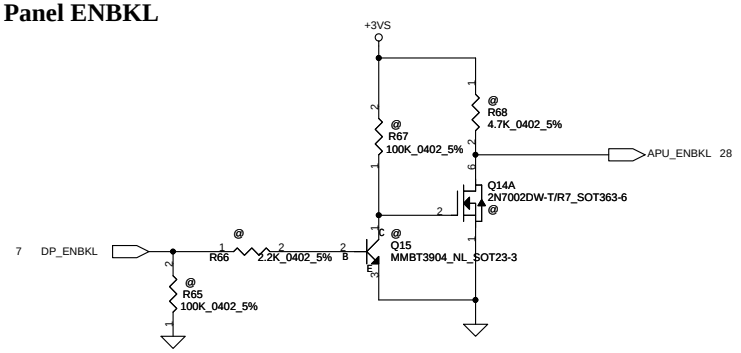
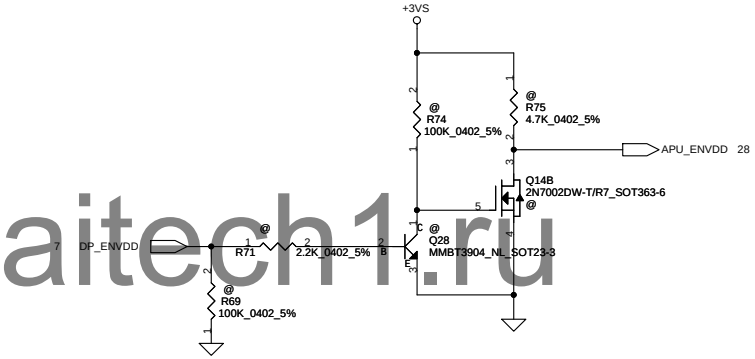
## HPD



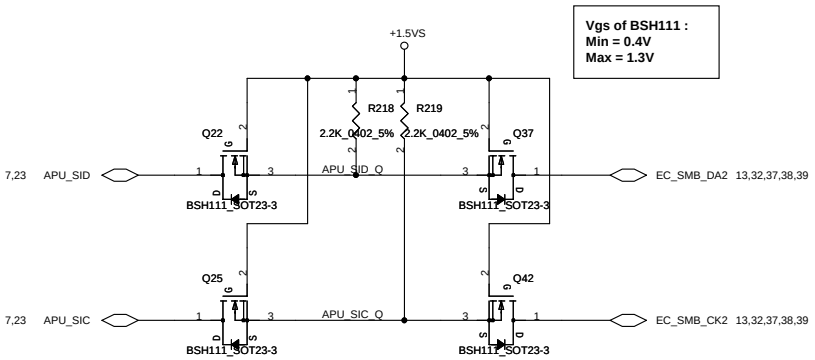

## Panel ENBKL



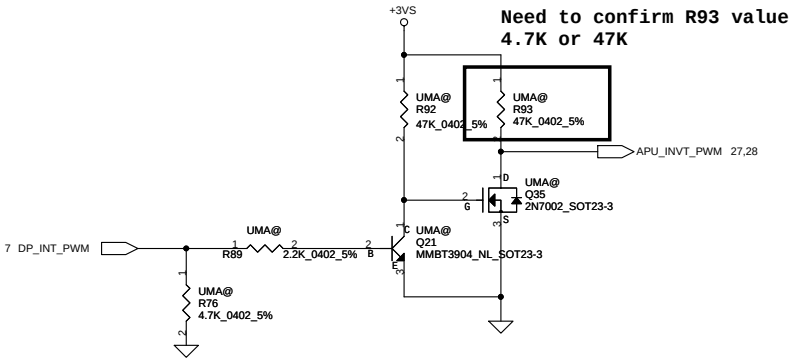

## Panel ENVDD




## SB-TSI




## Panel PWM

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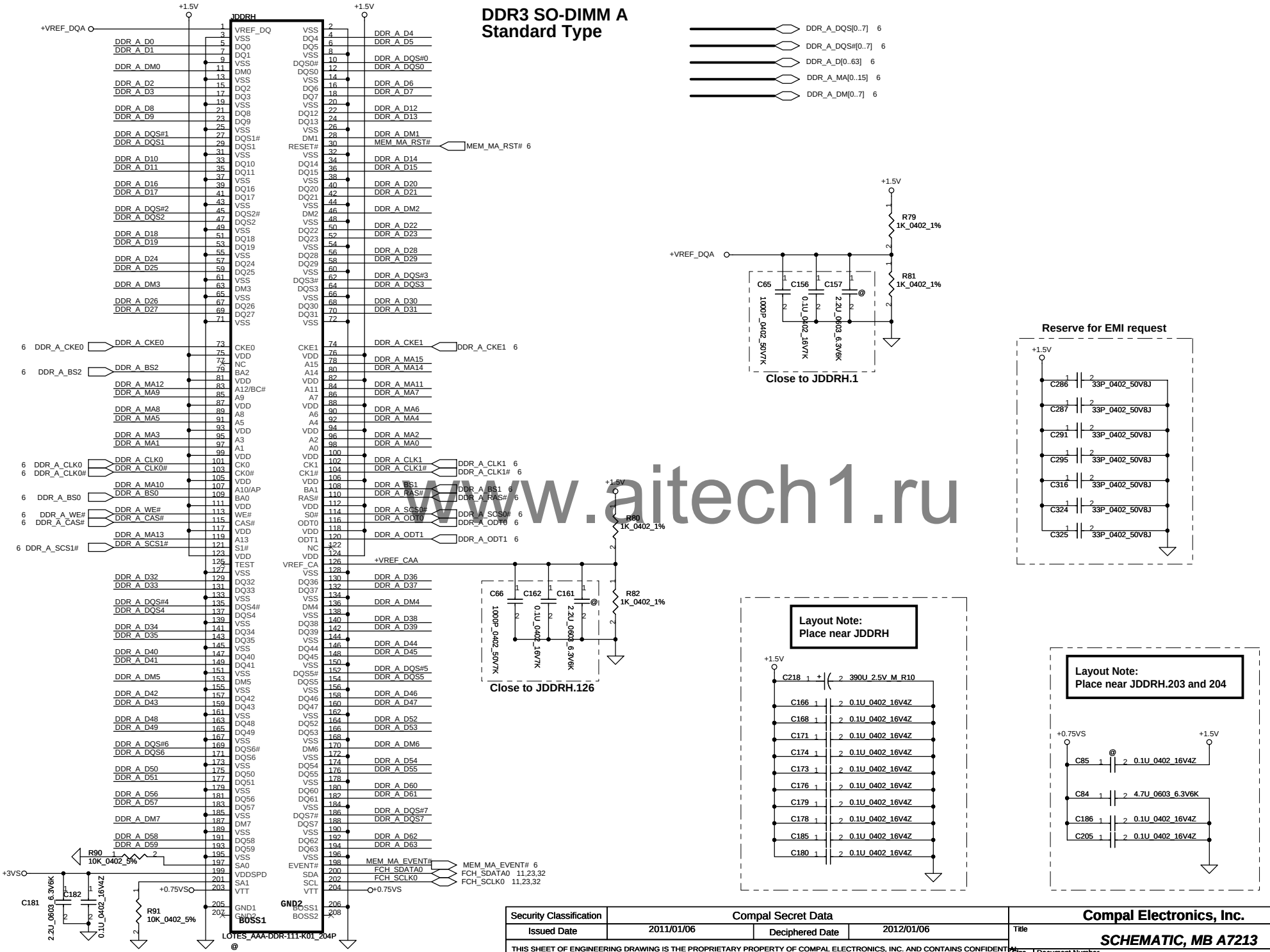
# DDR3 SO-DIMM A
# Standard Type




DDR_A_DQS[0..7] 6
DDR_A_DQS#[0..7] 6
DDR_A_D[0..63] 6
DDR_A_MA[0..15] 6
DDR_A_DM[0..7] 6

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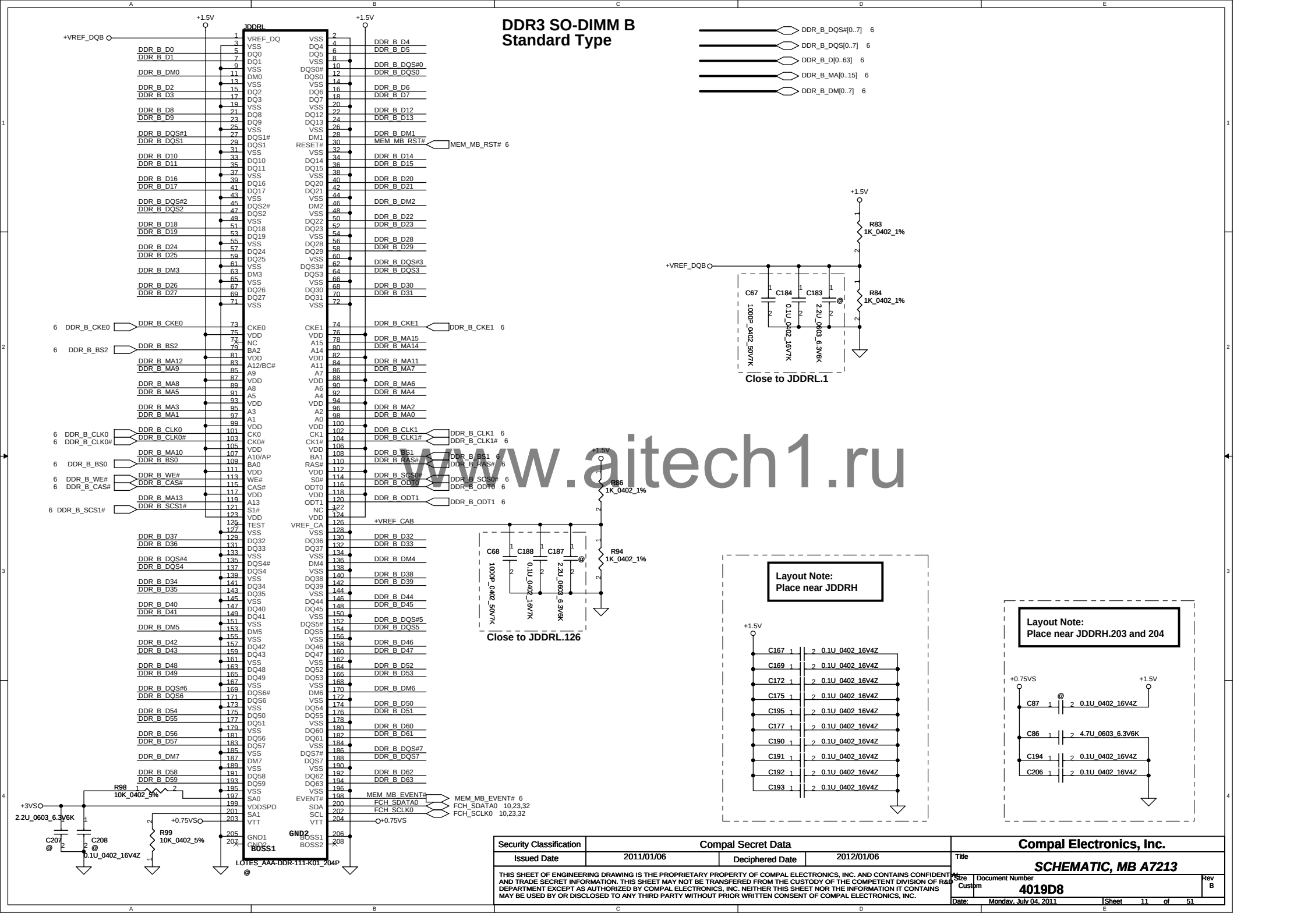
# DDR3 SO-DIMM B
# Standard Type

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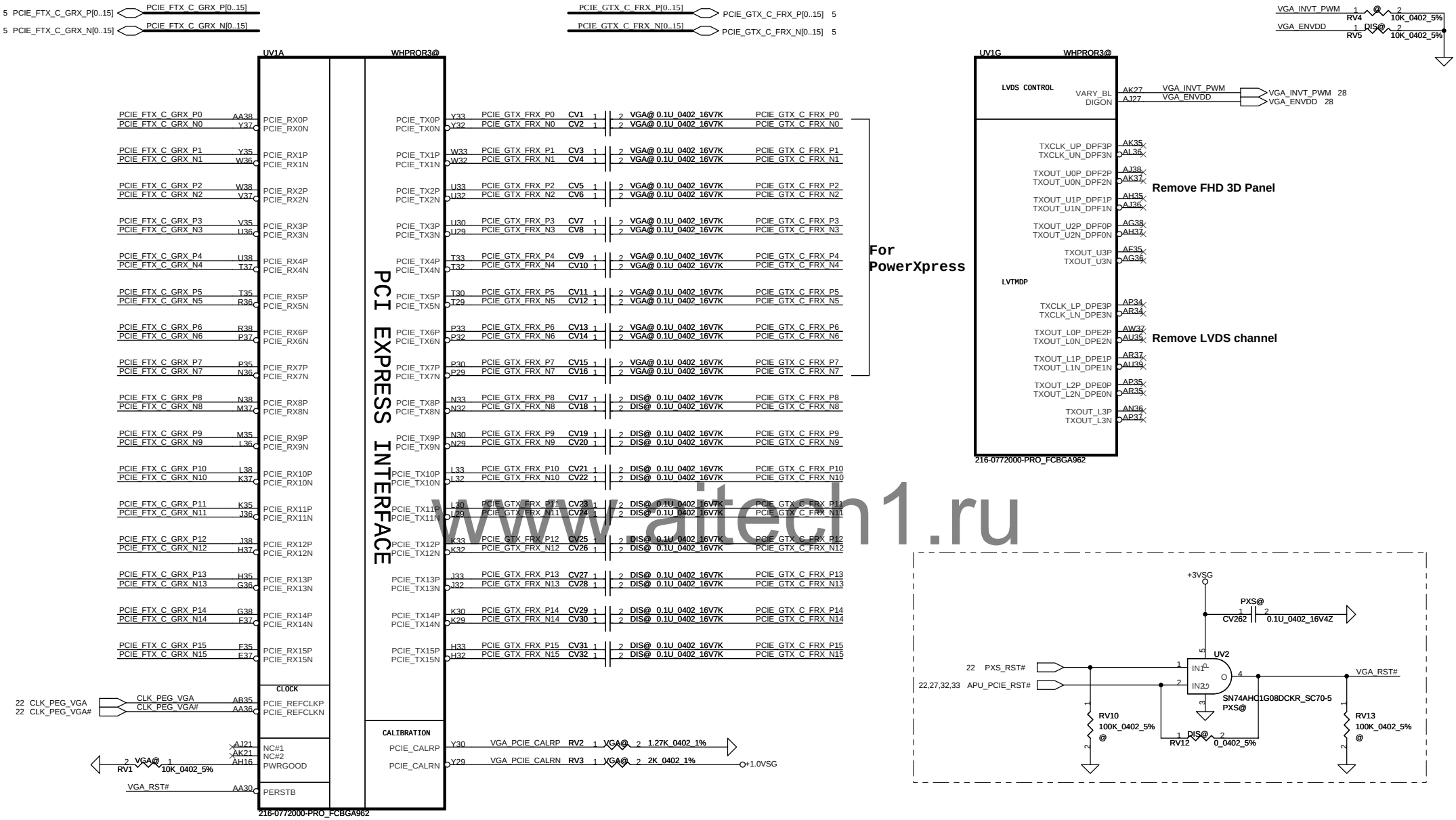


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| Strap Name | Pin Name | Pin Straps description <all internal PD> | Setting |
|---|---|---|---|
| VIP_DEVICE_EN_V2SYNC (GENLK_VSYNC) | GPIO9 | VIP Device Strap Enable indicates to the software driver (Internal PD)<br>0: Driver would ignore the value sampled on VHAD_0 during reset<br>1: VHAD_0 to determine whether or not a VIP slave device | 0 |
| VGA_DIS | GPIO9 | VGA Disable determines (Internal PD)<br>0: VGA Controller capacity enabled<br>1: The device will not be recognized as the system's VGA controller | 0 |
| TX_PWRS_ENB | GPIO0 | Transmitter Power Saving Enable (Internal PD)<br>0: 50% Tx output swing<br>1: full Tx output swing | 1 |
| TX_DEEMPH_EN | GPIO1 | PCI Express Transmitter De-emphasis Enable (Internal PD)<br>0: Tx de-emphasis diabled<br>1: Tx de-emphasis enabled | 1 |
| CONFIG[2]<br>CONFIG[1]<br>CONFIG[0] | GPIO13<br>GPIO12<br>GPIO11 | GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures<br>a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0]<br>b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 128 MB 000<br>256 MB 001 *<br>64 MB 010<br>32 MB 011 | 001 |
| BIOS_ROM_EN | GPIO22 | Enable external BIOS ROM device (Internal PD)<br>1: Enable 0: Diable | 0 |
| AUD[1]<br>AUD[0] | HSYNC<br>VSYNC | 00: No audio function; 10: Audio for DisplayPort only;<br>01: Audio for DisplayPort and HDMI if adapter is detected<br>11: Audio for both DisplayPort and HDMI | 11 |
| BIF_GEN2_EN | GPIO2 | 0= Advertises the PCI-E device as 2.5 GT/s capable at power-on<br>1= Advertises the PCI-E device as 5.0 GT/s capable at power-on<br>5.0 GT/s capability will be controlled by software | 0 |
| RESERVED | H2SYNC (GENLK_CLK)<br>GPIO8<br>GPIO21 | Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected | NC |

Don't have this strap for Whistler

Remove LVDS

Remove Thermal Interface

For 3D eDP Panel

Internal Thermal Sensor Address: 0x41 H

NC for Whistler

NC for Whistler
Except A2VSSQ change to TSVSSQ

Remove VGA_LCD_CLK/DATA

Close to GPU

For Debug

For DDR3/GDDR3

For GDDR5

For Capilano

For Capilano

VRAM STRAP

(VRAM_ID[0:3] internal pull-down)

| Location / VRAM | DDR3 Type | Part Number | VRAM_ID0 | VRAM_ID1 | VRAM_ID2 | VRAM_ID3 |
|---|---|---|---|---|---|---|
| Samsung (1GB) | 64Mx16 900MHz | K4W1G1646G-BC11 | 0 | 0 | 0 | 0 |
| HYNIX (1GB) | 64Mx16 900MHz | H5TQ1G63DFR-11C | 1 | 0 | 0 | 0 |
| Samsung (2GB) | 128Mx16 900MHz | K4W2G1646C-HC11 | 0 | 1 | 0 | 0 |
| HYNIX (2GB) | 128Mx16 900MHz | H5TQ2G63BFR-11C | 1 | 1 | 0 | 0 |

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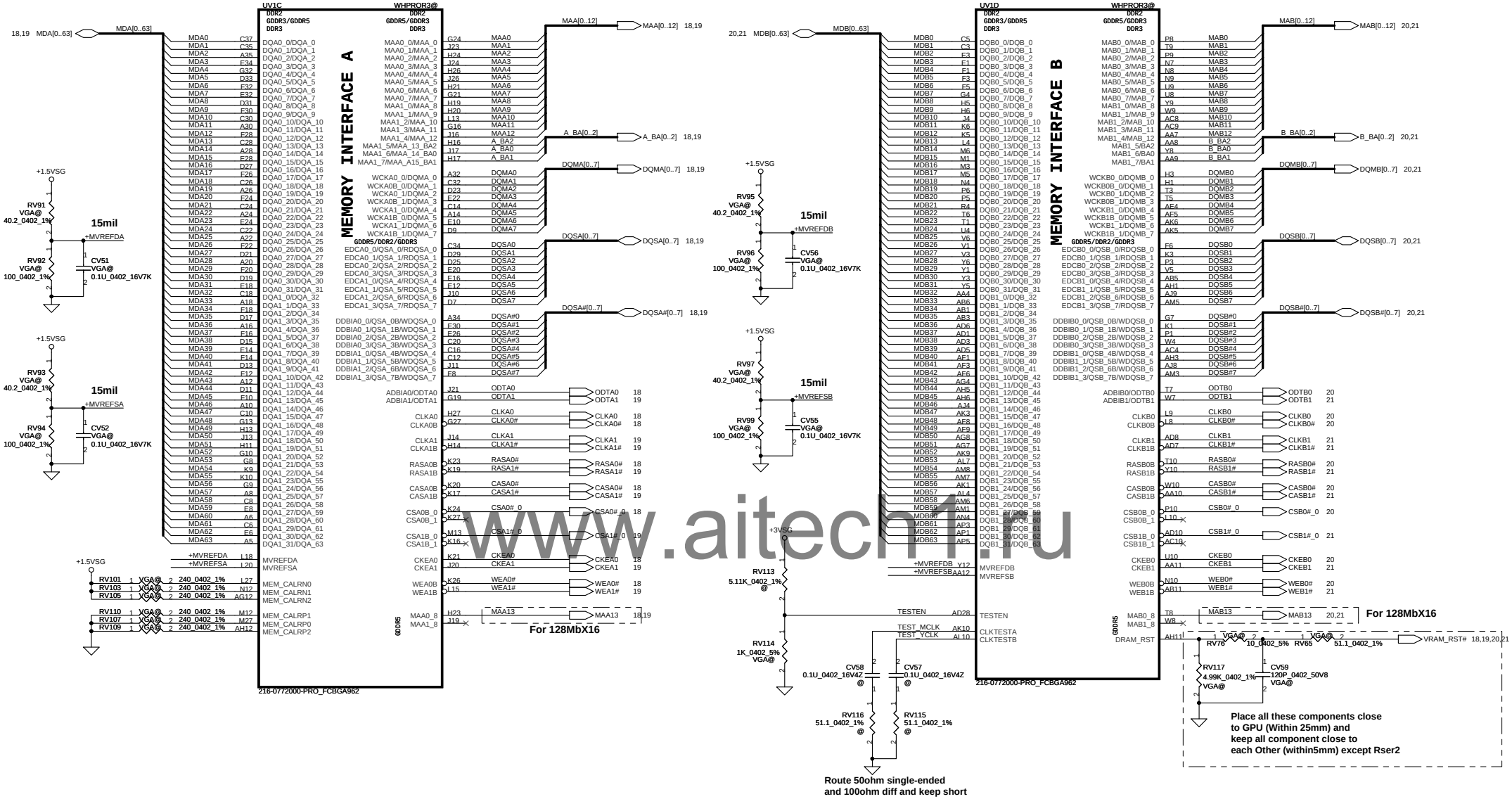


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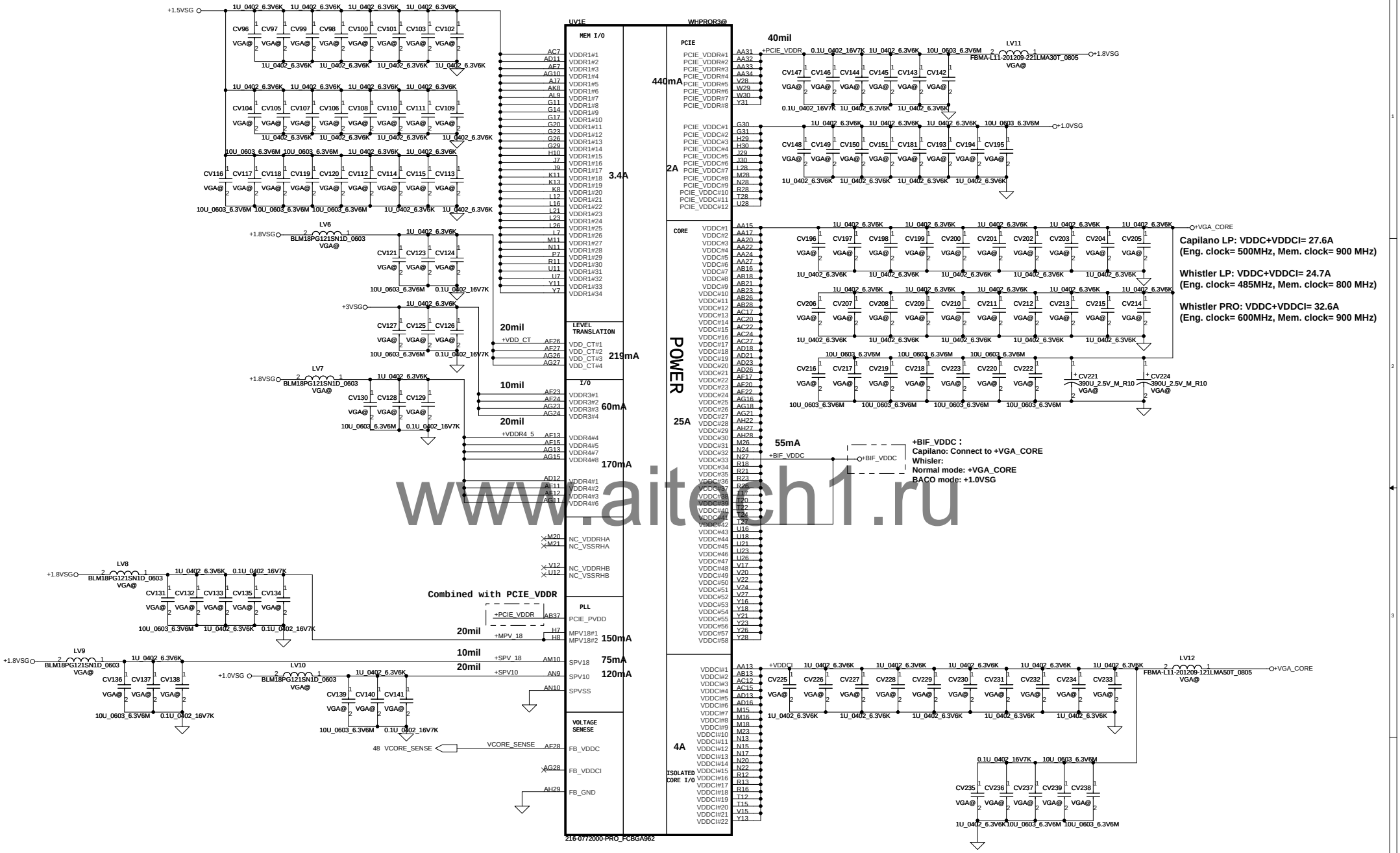


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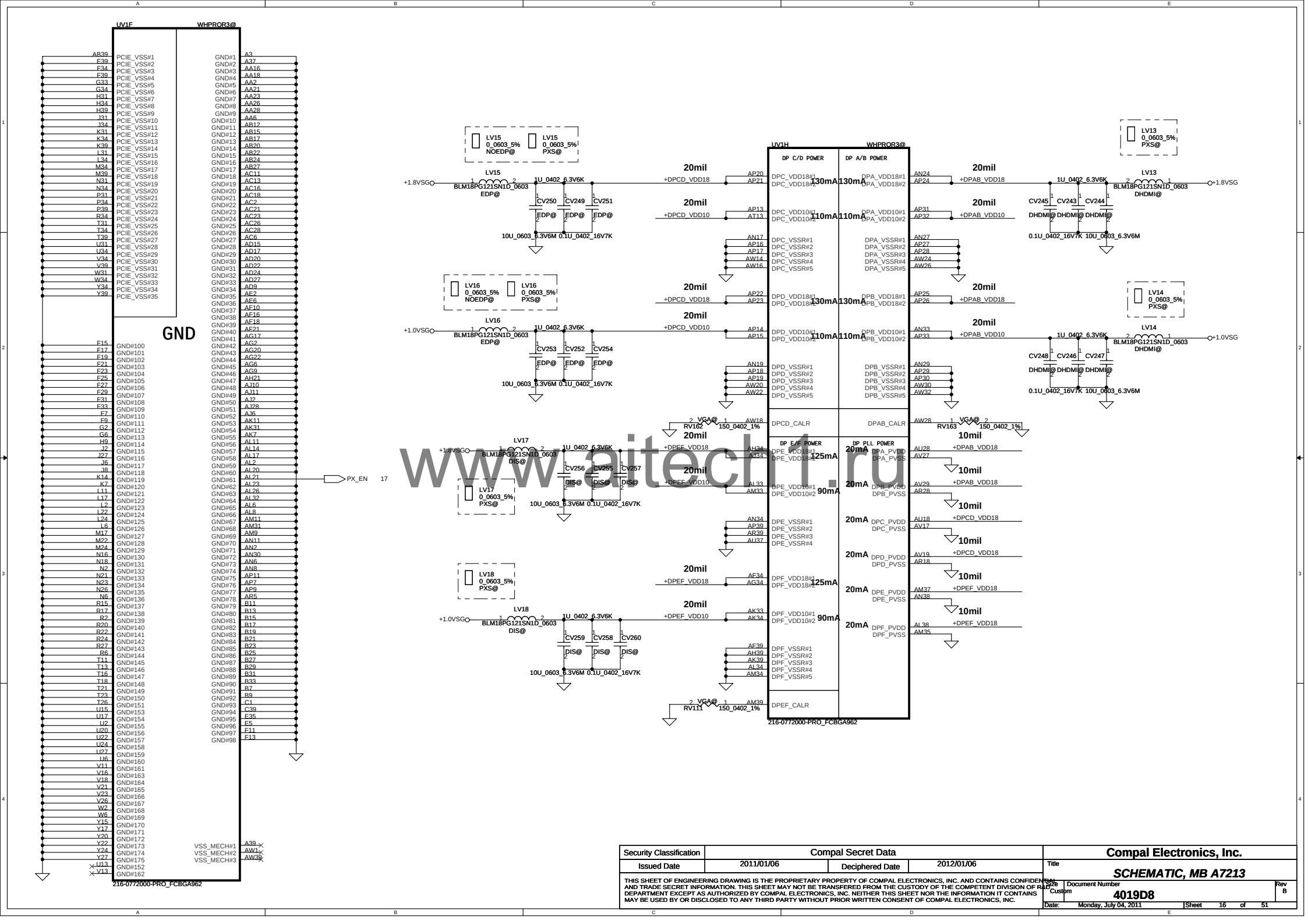


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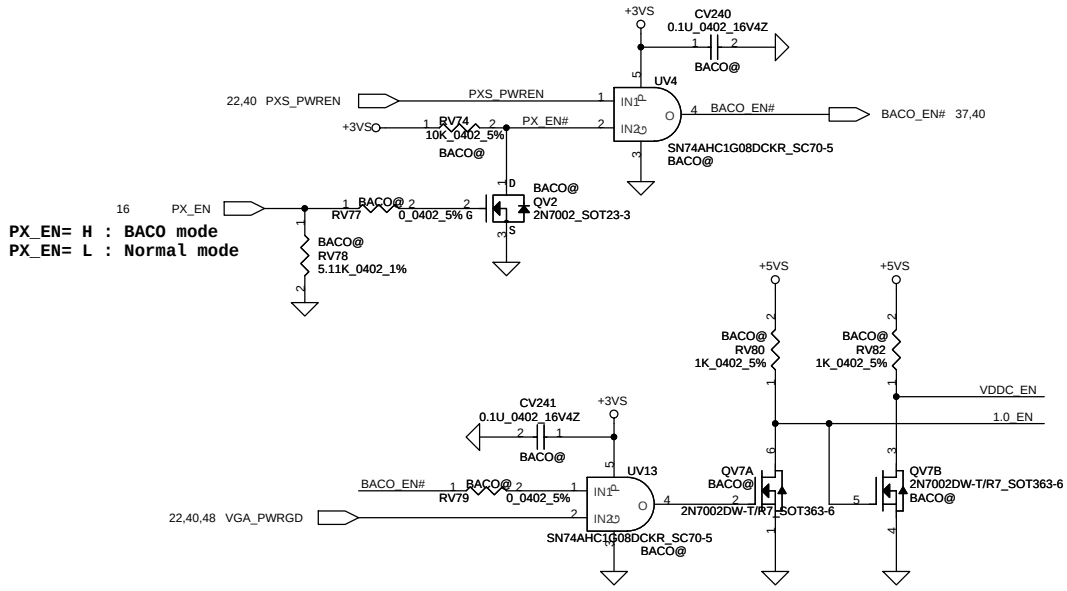


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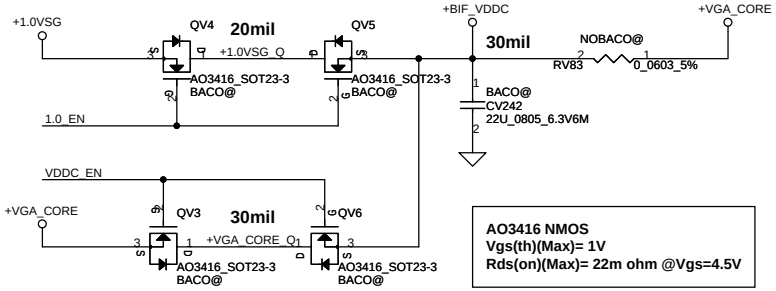
**BACO mode:**
**+VGA_CORE: off**
**+1.5VSG: off**
**+BIF_VDDC= +1.0VSG**

**Normal mode:**
**+BIF_VDDC= +VGA_CORE**




**AO3416 NMOS**
**Vgs(th)(Max)= 1V**
**Rds(on)(Max)= 22m ohm @Vgs=4.5V**

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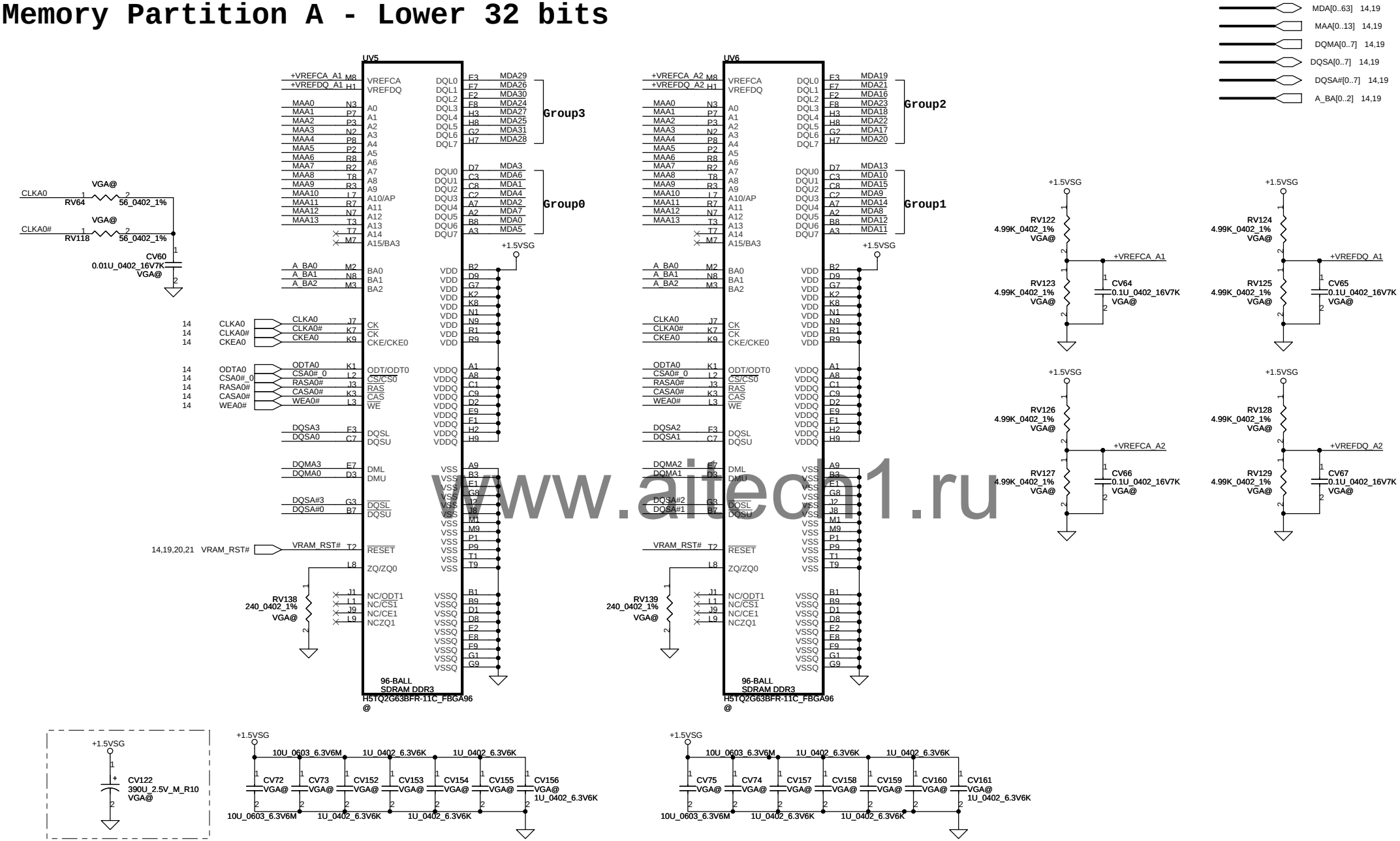
# Memory Partition A - Lower 32 bits

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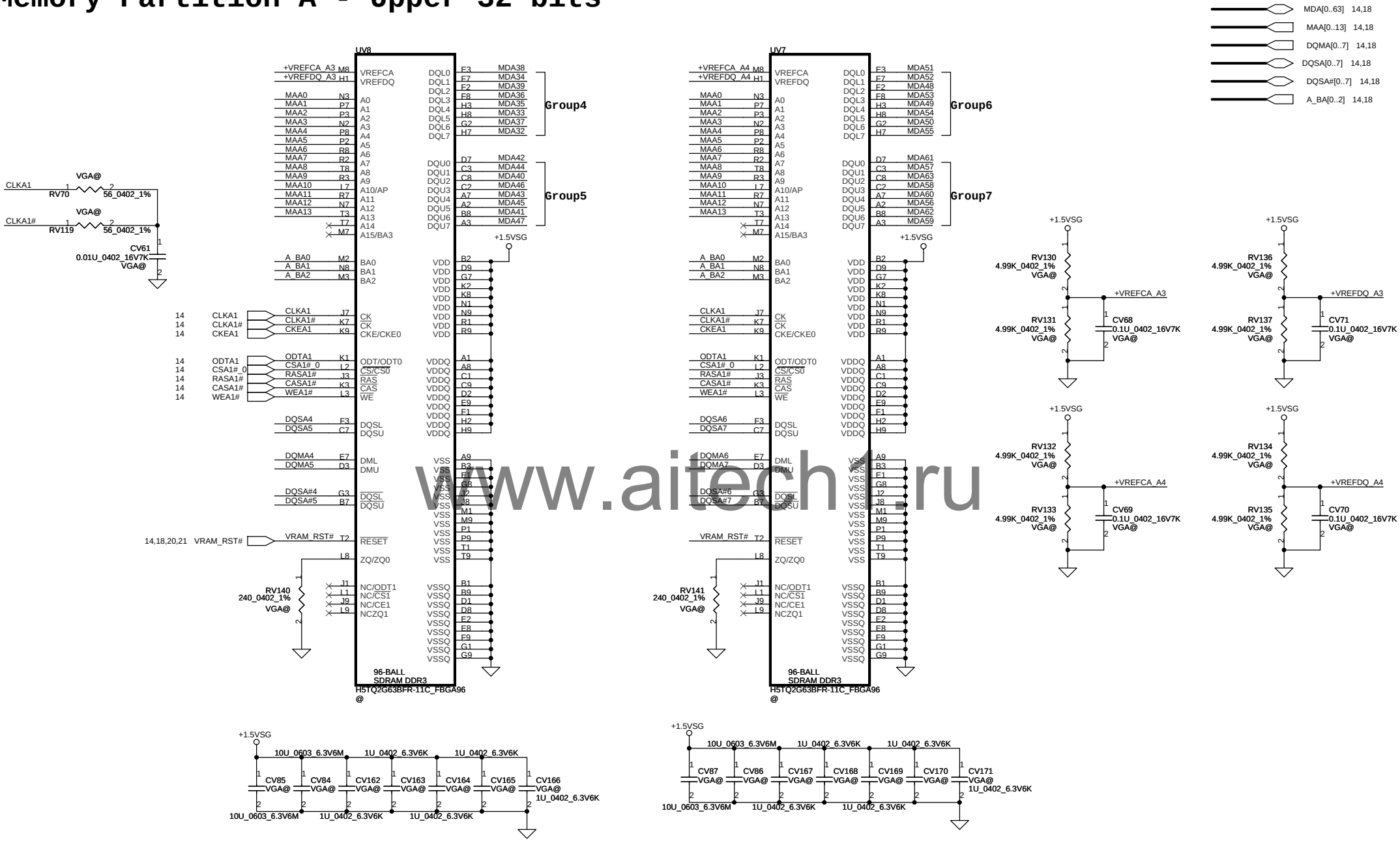
# Memory Partition A - Upper 32 bits

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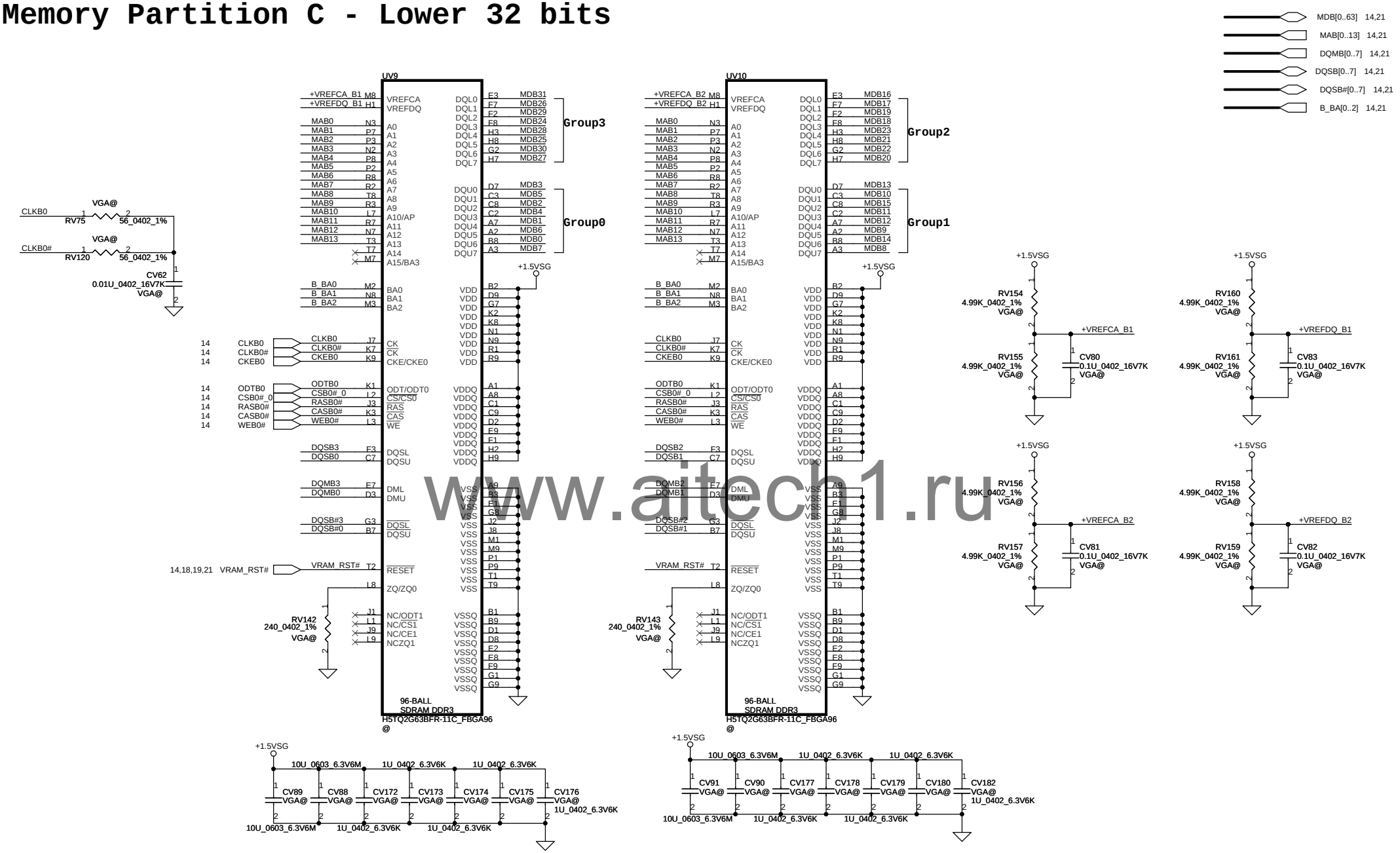
# Memory Partition C - Lower 32 bits

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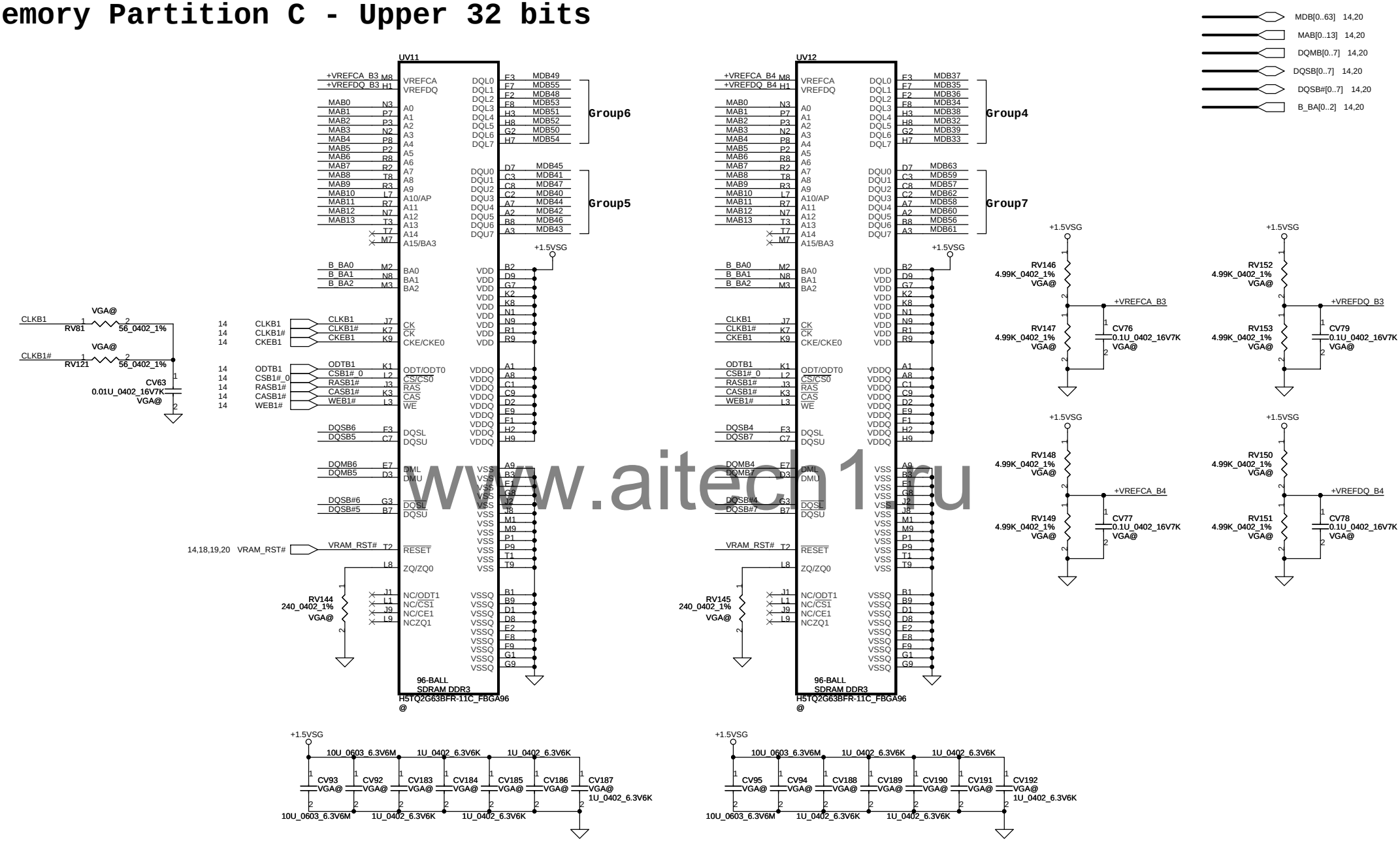
# Memory Partition C - Upper 32 bits

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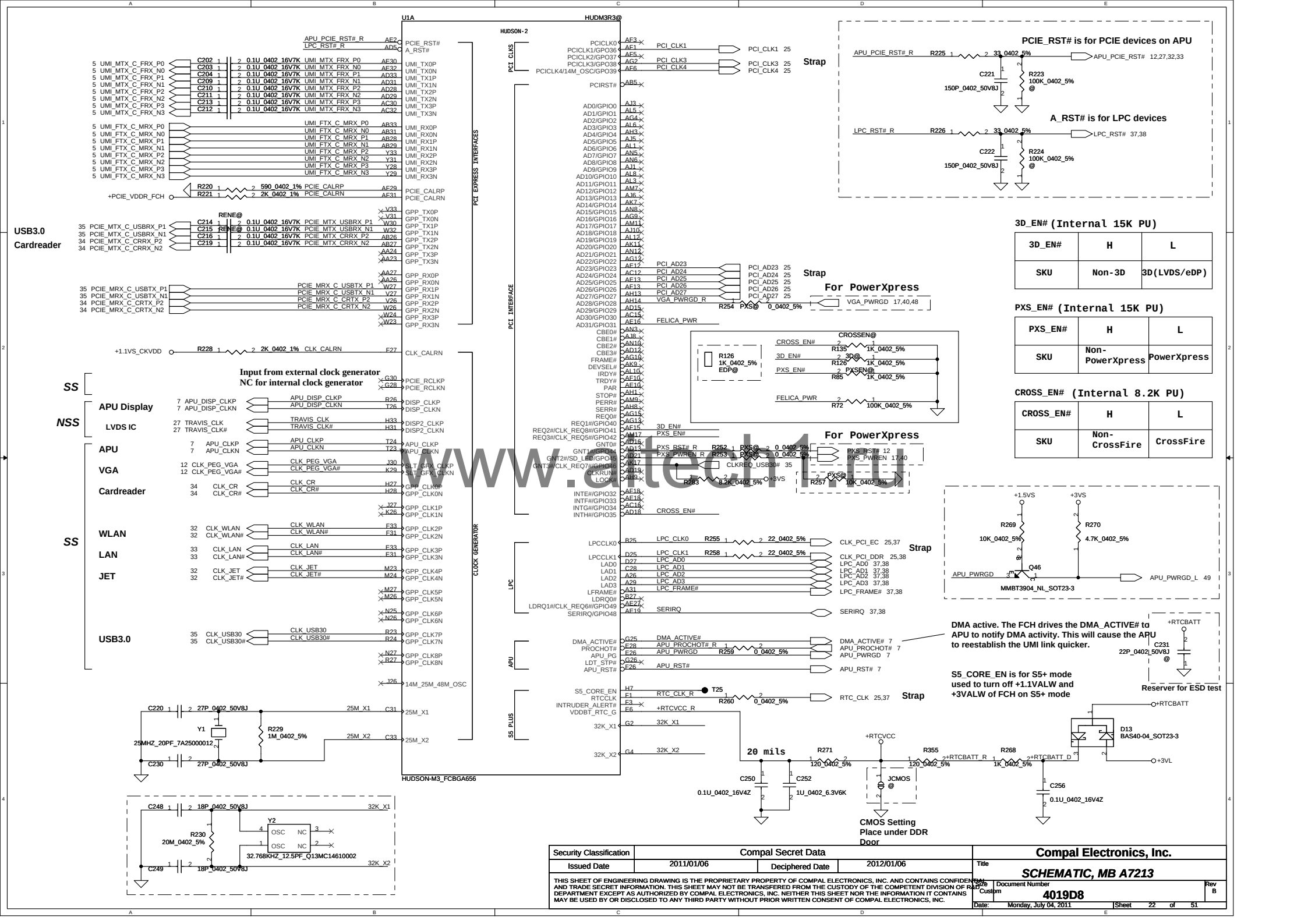


| 3D_EN# | H | L |
|---|---|---|
| SKU | Non-3D | 3D(LVDS/eDP) |

| PXS_EN# | H | L |
|---|---|---|
| SKU | Non-PowerXpress | PowerXpress |

| CROSS_EN# | H | L |
|---|---|---|
| SKU | Non-CrossFire | CrossFire |

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| | | | |
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PCIE_RST2# is for PCIE devices on FCH

U1D

HUDSON-2

HUDM3R3@

R227 2 @ 1 100K_0402_5%

C19 1 2 150P_0402_50V8J

R222 33_0402_5%

34,35 FCH_PCIE_RST#

37 EC_LID_OUT#

T68

37 SLP_S3#

37 SLP_S5#

37 PBTN_OUT#

37 FCH_PWRGD

T69

33,35 FCH_PCIE_WAKE#

T67

7 H_THERMTRIP#

+3VS R279 10K_0402_5%

37 EC_RSMRST#

33 CLKREQ_LAN#

D17 RB751V40_SC76-2

R361 0_0402_5%

32 CLKREQ_JET#

32 CLKREQ_LAN# R

CLKREQ_CR#

32 CLKREQ_WLAN#

T30

25 VGA_PD

R292 1 @ 2 0_0402_5% VGA_PD_FCH

T65

HDMI_HPD_FCH_R

13 PEG_CLKREQ#

+3VS R301 1 @ 2 8.2K_0402_5% PEG_CLKREQ#

2 VGA@ 1 R295 1K_0402_5%

SM Bus 0-->S0 PWR domain
SM Bus 1-->S5 PWR domain
(for ASF device only)

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off

Internal PU 10K

USB_OC1# is for USB port2

USB_OC0# is for USB port0 and port1

36 AZ_BITCLK_HD R320 1 2 33_0402_5% HDA_BITCLK

36 AZ_SDOUT_HD R321 1 2 33_0402_5% HDA_SDOUT

36 AZ_SDIN0_HD

36 AZ_SYNC_HD R322 1 2 33_0402_5% HDA_SYNC

36 AZ_RST_HD# R323 1 2 33_0402_5% HDA_RST#

35 USB30_SMI#

31 ODD_PLUGIN#

37 USB_OC3#

34 CR_CPPE#

32,35,37 USB_OC1#

31,37 USB_OC0#

+3VALW

R421 10K_0402_5% CR_CPPE#

R293 10K_0402_5% VGA_PD_FCH

R278 10K_0402_5% H_THERMTRIP#

R288 10K_0402_5% FCH_SCLK1

R289 10K_0402_5% FCH_SDATA1

R272 10K_0402_5% EC_LID_OUT#

R276 10K_0402_5% FCH_PCIE_WAKE#

REN@ R306 10K_0402_5% USB30_SMI#

R318 10K_0402_5% USB_OC0#

R319 10K_0402_5% USB_OC1#

R436 @ 330K_0402_5% ACIN_FCH#

R332 10K_0402_5% USB_OC3#

+3VS

R286 2.2K_0402_5% FCH_SCLK0

R287 2.2K_0402_5% FCH_SDATA0

R291 @ 8.2K_0402_5% CLKREQ_WLAN#

R290 @ 8.2K_0402_5% CLKREQ_JET#

R281 @ 8.2K_0402_5% CLKREQ_CR#

R282 1K_0402_5%

R284 @ 8.2K_0402_5% CLKREQ_LAN#_R

R280 100K_0402_5% EC_RSMRST#

R324 @ 10K_0402_5% HDA_BITCLK

R325 @ 10K_0402_5% AZ_SDIN0_HD

Set cardreader clock as free-running

CIR@ R442 1K_0402_5%

T26 T27 CIR_EN#

ACIN_FCH#

Change to low active for AC_IN LED issue

13,37,39,43 ACIN

Q191 2N7002_SOT23-3

PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166

PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

HUDSON-M3_FCBGA656

For FCH internal debug use (Internal 10K pull-down)

+3VALW R273 @ 2.2K_0402_5% TEST0

R274 @ 2.2K_0402_5% TEST1

R275 @ 2.2K_0402_5% TEST2

CEC@ Q192 2N7002_SOT23-3

9,30 HDMI_HPD

R331 10K_0402_5% @

R419 CEC@ 0_0402_5% HDMI_HPD_FCH_R

ACPI / WAKE UP EVENTS

GPIO

USB OC

HD AUDIO

USB MISC

USB 1.1

USB 2.0

USB 3.0

EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC

USB_RCOMP R329 1 2 11.8K_0402_1%

USB_FSD1P/GPIO186
USB_FSD1N

USB_FSD0P/GPIO185
USB_FSD0N

USB_HSD13P
USB_HSD13N

USB_HSD12P
USB_HSD12N

USB_HSD11P
USB_HSD11N

USB_HSD10P
USB_HSD10N

USB_HSD9P
USB_HSD9N

USB_HSD8P
USB_HSD8N

USB_HSD7P
USB_HSD7N

USB_HSD6P
USB_HSD6N

USB_HSD5P
USB_HSD5N

USB_HSD4P
USB_HSD4N

USB_HSD3P
USB_HSD3N

USB_HSD2P
USB_HSD2N

USB_HSD1P
USB_HSD1N

USB_HSD0P
USB_HSD0N

USBSS_CALRP R330 1 M3@ 2 1K_0402_1%

USBSS_CALRN R334 1 M3@ 2 1K_0402_1%

+VDDANCR_11_SSUSB

USB_SS_TX3P
USB_SS_TX3N

USB_SS_RX3P
USB_SS_RX3N

USB_SS_TX2P
USB_SS_TX2N

USB_SS_RX2P
USB_SS_RX2N

USB_SS_TX1P
USB_SS_TX1N

USB_SS_RX1P
USB_SS_RX1N

USB_SS_TX0P
USB_SS_TX0N

USB_SS_RX0P
USB_SS_RX0N

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

R326 10K_0402_5% +3VALW

R328 10K_0402_5%

FCH_SIC

FCH_SID R338 0_0402_5% APU_SIC 7,9

R343 0_0402_5% APU_SID 7,9

SB-TSI

EC_PWM2 EC_PWM2 25

Strap

Hudson-M2/M3
OHCI (DEV-20, FUN-5)

Hudson-M2
OHCI (DEV-22, FUN-0)
EHCI (DEV-22, FUN-2)

Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

USB 3.0
(For Hudson M3 only)

Remove Felica

WLAN (BT)

Remove Finger Printer

Hudson-M2/M3
OHCI (DEV-19, FUN-0)
EHCI (DEV-19, FUN-2)

Remove 3G/TV #1

Int. Camera

Remove TV #2

USB-Left

USB-Right2

USB-Right1

Hudson-M2/M3
OHCI (DEV-18, FUN-0)
EHCI (DEV-18, FUN-2)

<Support Wakeup>

Hudson-M3
XHCI (DEV-16, FUN-0)
XHCI (DEV-16, FUN-1)

USB 3.0
(For Hudson M3 only)

Place R425 and C363 close to FCH for ESD

+3VALW R312 10K_0402_5% @

+3VS R311 10K_0402_5%

Q208 2N7002_SOT23-3

ODD_DA# FCH R425 0_0402_5% ODD_DA# Q

C379 0.1U_0402_16V4Z

ODD_DA# 31

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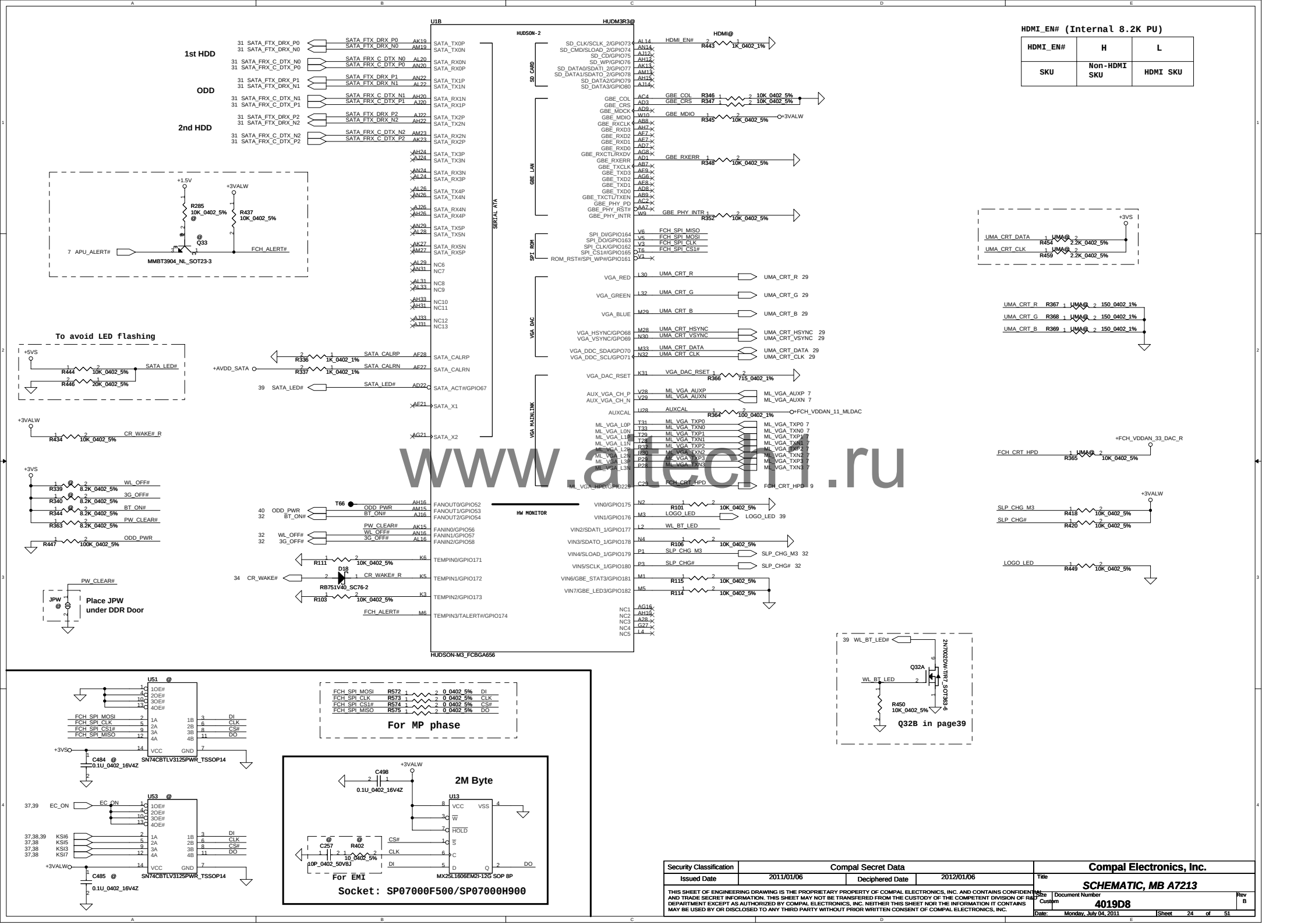


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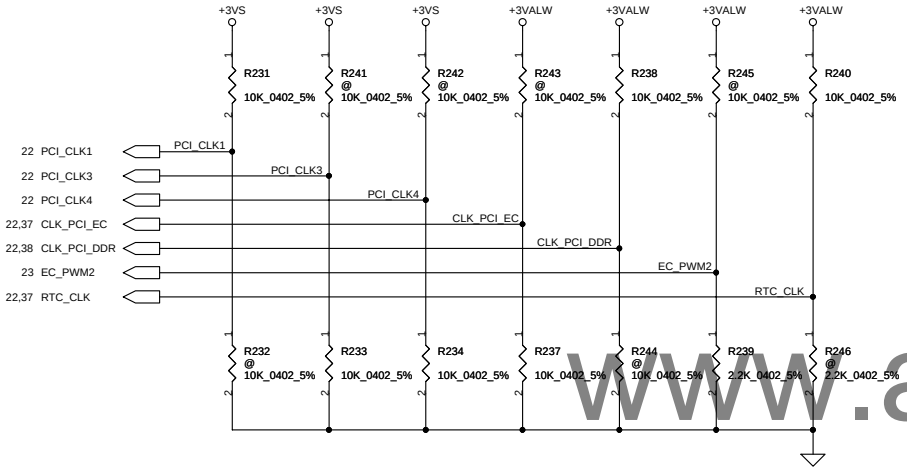
## STRAP PINS

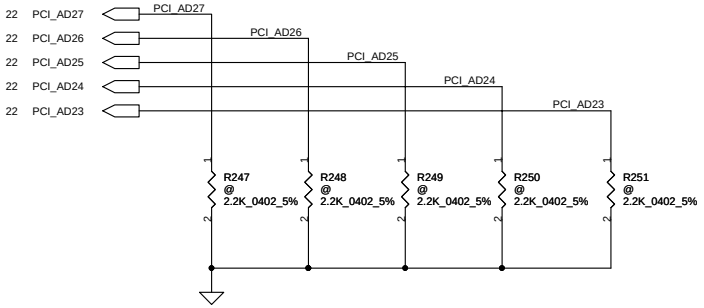
| | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | EC_PWM2 | RTC_CLK |
|---|---|---|---|---|---|---|---|
| PULL HIGH | ALLOW PCIE GEN2 DEFAULT | ENABLE DEBUG STRAP | NON_FUSION CLOCK MODE | EC ENABLED | CLKGEN ENABLED DEFAULT | LPC ROM (INTERNAL 10K PULL-UP) | S5 PLUS MODE DISABLED DEFAULT |
| PULL LOW | FORCE PCIE GEN1 | DISABLE DEBUG STRAP DEFAULT | FUSION CLOCK MODE DEFAULT | EC DISABLED DEFAULT | CLKGEN DISABLE | SPI ROM DEFAULT | S5 PLUS MODE ENABLED |



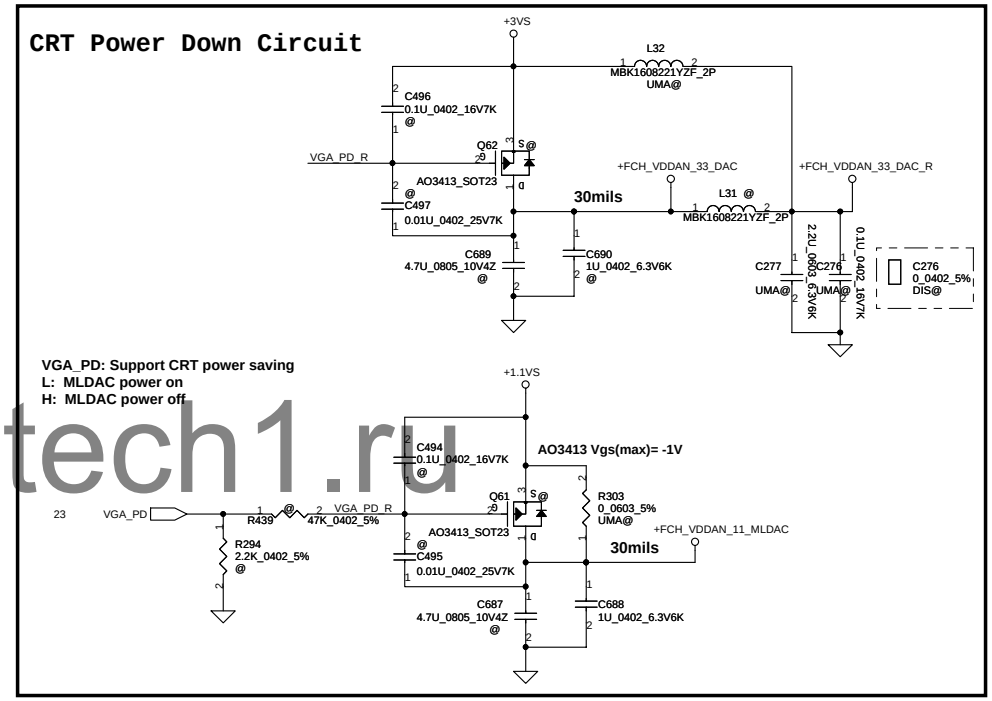

## DEBUG STRAPS

**FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]**

| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|
| PULL HIGH | USE PCI PLL DEFAULT | DISABLE ILA AUTORUN DEFAULT | USE FC PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | ENABLE ILA AUTORUN | BYPASS FC PLL | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |




## CRT Power Down Circuit

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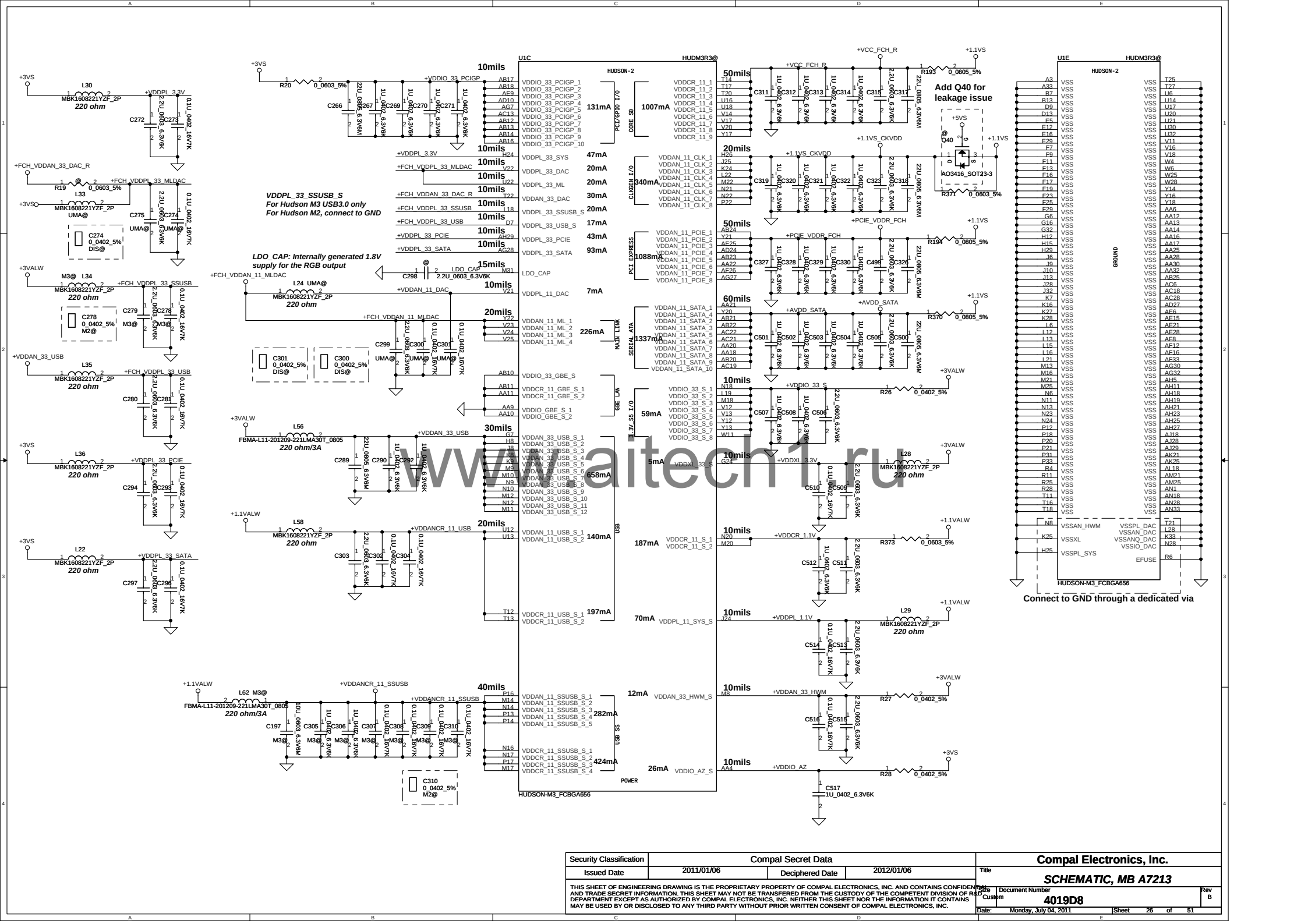


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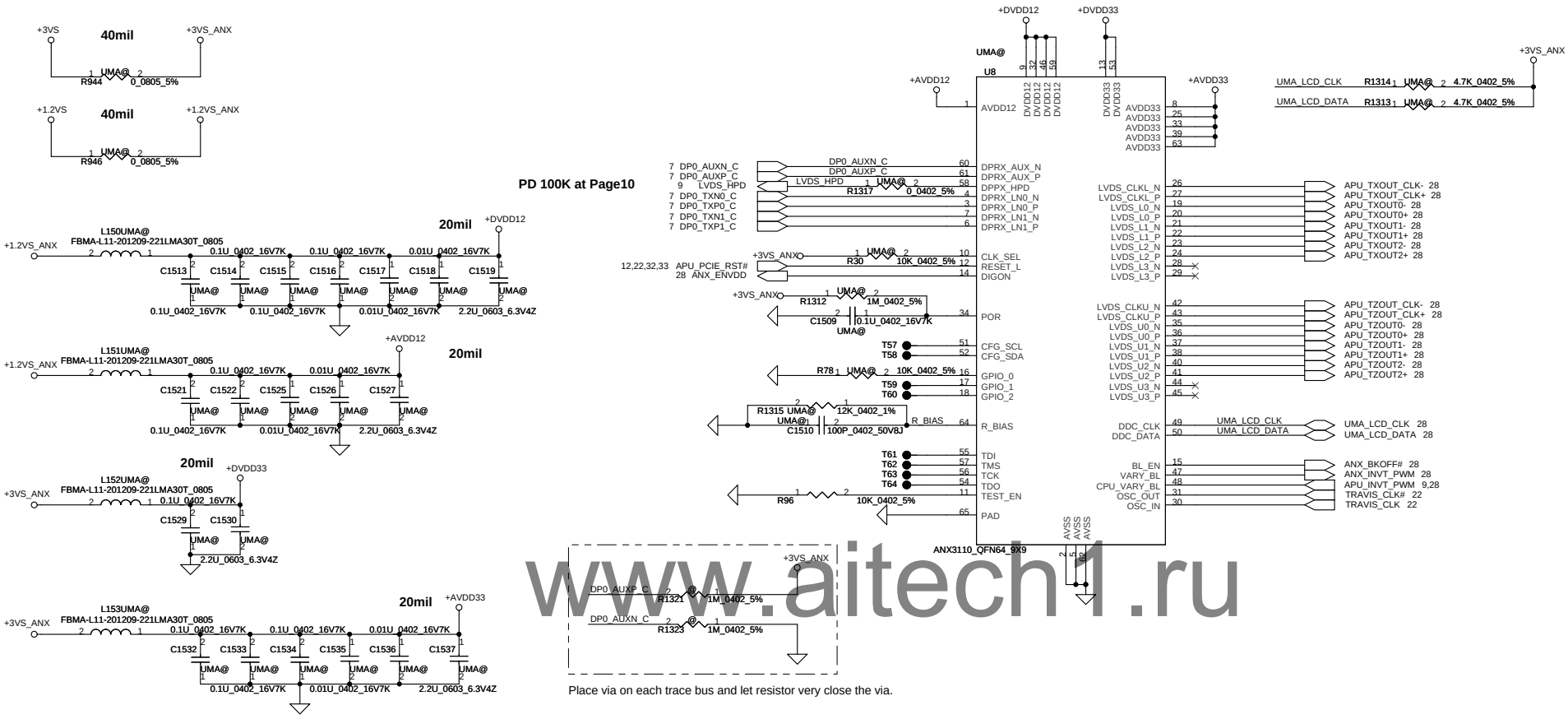


Place via on each trace bus and let resistor very close the via.

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|---|---|---|
| Custom | 4019D8 | B |

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## For UMA & PowerXpress

27 APU_TXOUT0+ — RD262 UMA@ 0_0402_5% — LVDS_TXOUT0+
27 APU_TXOUT0- — RD263 UMA@ 0_0402_5% — LVDS_TXOUT0-
27 APU_TXOUT1+ — RD265 UMA@ 0_0402_5% — LVDS_TXOUT1+
27 APU_TXOUT1- — RD264 UMA@ 0_0402_5% — LVDS_TXOUT1-
27 APU_TXOUT2+ — RD298 UMA@ 0_0402_5% — LVDS_TXOUT2+
27 APU_TXOUT2- — RD277 UMA@ 0_0402_5% — LVDS_TXOUT2-
27 APU_TXOUT_CLK+ — RD297 UMA@ 0_0402_5% — LVDS_TXCLK+
27 APU_TXOUT_CLK- — RD296 UMA@ 0_0402_5% — LVDS_TXCLK-
27 APU_TZOUT0+ — RD268 UMA@ 0_0402_5% — LVDS_TZOUT0+
27 APU_TZOUT0- — RD267 UMA@ 0_0402_5% — LVDS_TZOUT0-
27 APU_TZOUT1+ — RD269 UMA@ 0_0402_5% — LVDS_TZOUT1+
27 APU_TZOUT1- — RD266 UMA@ 0_0402_5% — LVDS_TZOUT1-
27 APU_TZOUT2+ — RD302 UMA@ 0_0402_5% — LVDS_TZOUT2+
27 APU_TZOUT2- — RD278 UMA@ 0_0402_5% — LVDS_TZOUT2-
27 APU_TZOUT_CLK+ — RD301 UMA@ 0_0402_5% — LVDS_TZCLK+
27 APU_TZOUT_CLK- — RD303 UMA@ 0_0402_5% — LVDS_TZCLK-
27 UMA_LCD_CLK — RD300 UMA@ 0_0402_5% — LVDS_EDID_CLK
27 UMA_LCD_DATA — RD299 UMA@ 0_0402_5% — LVDS_EDID_DATA
9,27 APU_INVT_PWM — RD332 @ 0_0402_5% — LED_PWM
9 APU_ENVDD — RD350 @ 0_0402_5% — LCD_ENVDD
9 APU_ENBKL — RD357 @ 0_0402_5% — EC_ENBKL — EC_ENBKL 37

Close to LVDS Connector

## To prevent EC pin damage

LED_PWM — RD449 @ 0_0402_5% — DD29 RB751V40_SC76-2 — LED_PWM_D — RD144 47K_0402_5%
37 BKOFF# — DD30 RB751V40_SC76-2 — BKOFF#_D — RD113 10K_0402_5%

## Reserve for EMI request

23 USB20_N5 — RD78 CAM@ 0_0402_5% — LD55 @ — USB20_N5_R
23 USB20_P5 — WCM-2012-900T_0805 — USB20_P5_R
RD96 CAM@ 0_0402_5%

## EC PWM

37 INVT_PWM — RD387 @ 0_0402_5% — LED_PWM

+LCD_VDD, +3VS, +5VS

RD107 150_0603_5% UMA@ — QD1A UMA@ 2N7002DW-T/R7_SOT363-6
RD108 100K_0402_5% UMA@
RD120 100K_0402_5% EDP@
RD109 47K_0402_5% UMA@ — LCDPWR_GATE
LCD_ENVDD — QD1B 2N7002DW-T/R7_SOT363-6 UMA@
RD112 100K_0402_5% UMA@

UMA@ CD228 0.1U_0402_16V7K — QD17 AO3413_SOT23 — W=80mils
CD229 0.01U_0402_25V7K UMA@
CD233 0.1U_0402_16V4Z UMA@ — W=80mils

EDP@ CD251 0.1U_0402_16V7K — QD23 AO3413_SOT23 — W=80mils
+LCD_VDD — W=80mils

RD107 150_0603_5% EDP@ — RD109 47K_0402_5% EDP@ — CD233 0.1U_0402_16V4Z EDP@
CD229 0.01U_0402_25V7K EDP@ — QD1 2N7002DW-T/R7_SOT363-6 EDP@

RD107 150_0603_5% NO3D@ — RD108 100K_0402_5% NO3D@ — RD109 47K_0402_5% NO3D@ — CD228 0.1U_0402_16V7K NO3D@
QD1 2N7002DW-T/R7_SOT363-6 NO3D@ — CD229 0.01U_0402_25V7K NO3D@ — CD233 0.1U_0402_16V4Z NO3D@
QD17 AO3413_SOT23 NO3D@

## For DISCRETE

Remove LVDS channel

12 VGA_INVT_PWM — RD349 DIS@ 0_0402_5% — LED_PWM
12 VGA_ENVDD — RD355 DIS@ 0_0402_5% — LCD_ENVDD
13 VGA_ENBKL — RD358 DIS@ 0_0402_5% — EC_ENBKL

Close to LVDS Connector

**Remove DISCRETE for 3D LVDS Panel**

**Remove 3D LVDS Panel**

## DISCRETE for 3D eDP Panel

13 VGA_EDP_TX0+ — CD880 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT0+
13 VGA_EDP_TX0- — CD881 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT0-
13 VGA_EDP_TX1+ — CD882 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT1+
13 VGA_EDP_TX1- — CD883 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT1-
13 VGA_EDP_TX2+ — CD884 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT2+
13 VGA_EDP_TX2- — CD885 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT2-
13 VGA_EDP_TX3+ — CD886 EDP@ 0.1U_0402_16V7K — LVDS_TXCLK+
13 VGA_EDP_TX3- — CD887 EDP@ 0.1U_0402_16V7K — LVDS_TXCLK-

Close to LVDS1 Connector

13 VGA_EDP_AUX+ — CD888 EDP@ 0.1U_0402_16V7K — LVDS_EDID_CLK
13 VGA_EDP_AUX- — CD889 EDP@ 0.1U_0402_16V7K — LVDS_EDID_DATA

Close to LVDS Connector

## LCD/PANEL BD. Conn.

+3VS — RD388 CAM@ 0_0603_5% — +3VS_LVDS_CAM — CD225 CAM@ 0.1U_0402_16V4Z — JLVDS @ ACES_87242-0041-09

USB20_P5_R, USB20_N5_R
LVDS_TXOUT0+, LVDS_TXOUT0-, LVDS_TXOUT1+, LVDS_TXOUT1-, LVDS_TXOUT2+, LVDS_TXOUT2-
LVDS_TZOUT0+, LVDS_TZOUT0-, LVDS_TZOUT1+, LVDS_TZOUT1-, LVDS_TZOUT2+, LVDS_TZOUT2-
BKOFF# D
LVDS_TXCLK+, LVDS_TXCLK-, LVDS_TZCLK+, LVDS_TZCLK-
LVDS_EDID_CLK, LVDS_EDID_DATA, INT_MIC_CLK, INT_MIC_DATA, LCD_ENVDD, LED_PWM_D, +3VS_LVDSDDC
GMD GND

DD84 YSLC05CH_SOT23-3
INT_MIC_CLK 36
INT_MIC_DATA 36

3A
+LCD_VDD — CD226 0.1U_0402_16V4Z — CD227 4.7U_0805_10V4Z
+LCD_INV

W=20mils

RD1440 0_0603_5% UMA@
+3VS_LVDSDDC — RD143 EDP@ 0_0402_5% — EDP_HPD 13
RD1440 NOEDP@ 0_0603_5% — +3VS

For EMI
CD231 @ 680P_0402_50V7K — NOEDP@ CD232 0.1U_0402_16V4Z
CD232 0.1U_0402_16V4Z UMA@

+LCD_INV — LD2 FBMA-L11-201209-221LMA30T_0805 — B+
CD234 68P_0402_50V8J — CD235 0.1U_0402_25V6

For EMI
B+
CD235 @ — CD263 @ — CD489 @ — CD490 @ — 0.1U_0402_25V6

+3VS
EDP@ RD209 100K_0402_5% — LVDS_EDID_DATA
EDP@ RD256 100K_0402_5% — LVDS_EDID_CLK

## For LVDS Translator

27 ANX_INVT_PWM — RD333 UMA@ 0_0402_5% — LED_PWM
27 ANX_ENVDD — RD351 UMA@ 0_0402_5% — LCD_ENVDD
27 ANX_BKOFF# — RD360 UMA@ 0_0402_5% — EC_ENBKL

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| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019D8 | B |

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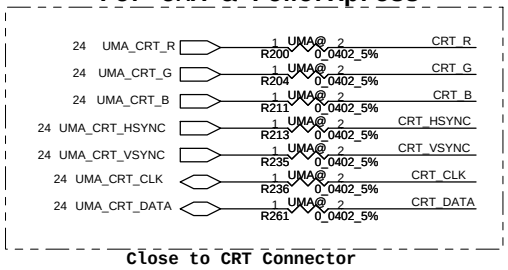
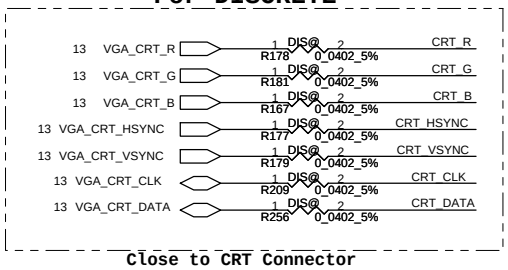
# CRT CONNECTOR

## For UMA & PowerXpress

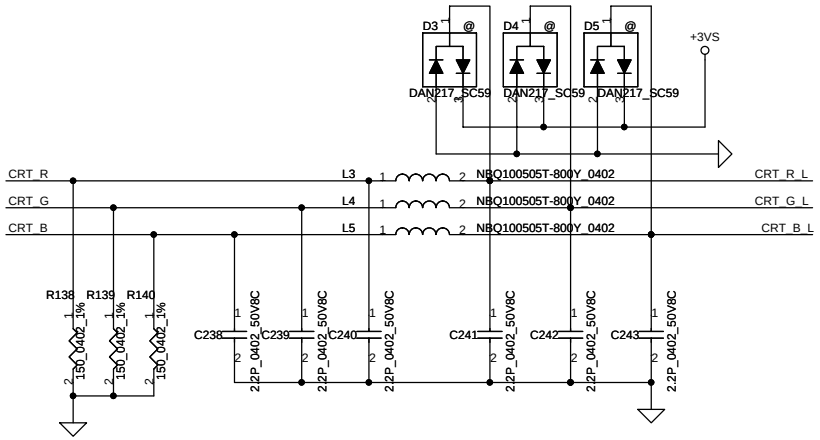


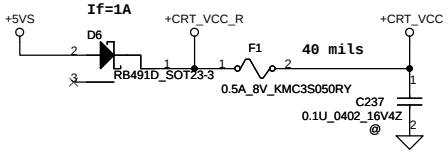

**Close to CRT Connector**

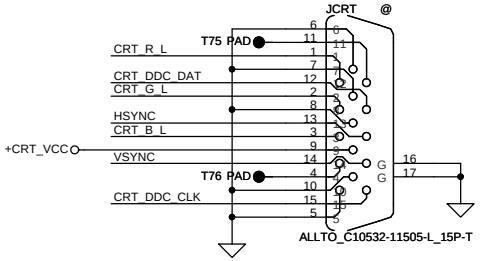
## For DISCRETE

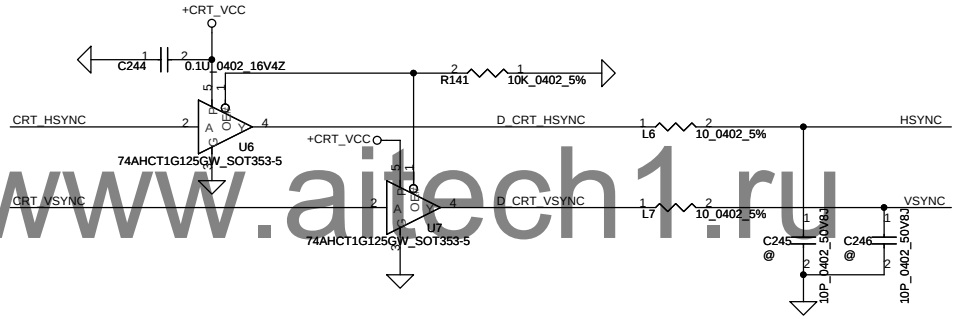


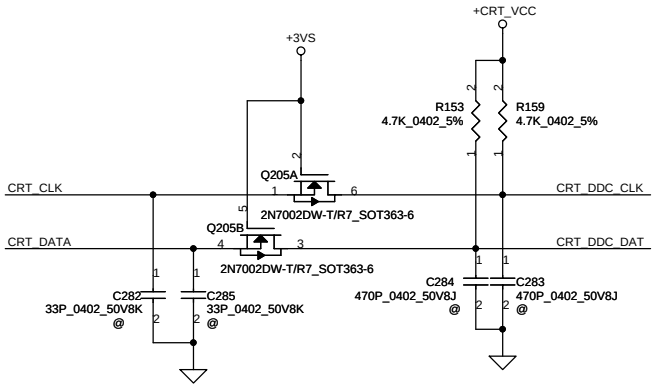

**Close to CRT Connector**

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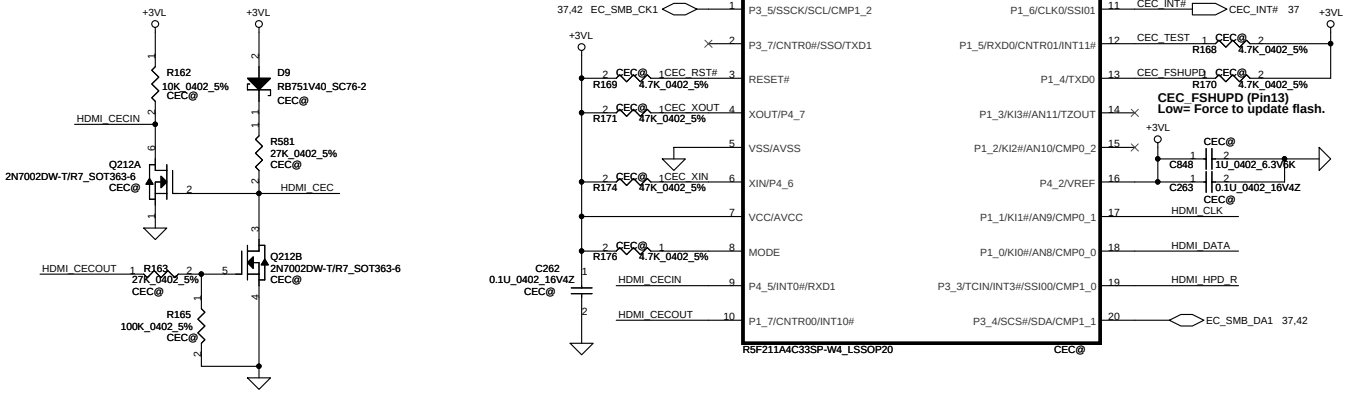
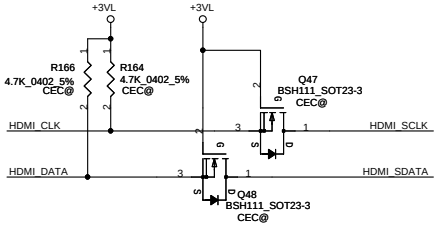
# HDMI CEC Controller



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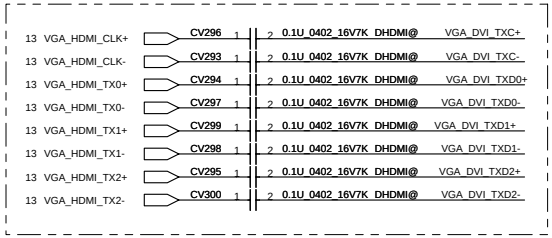

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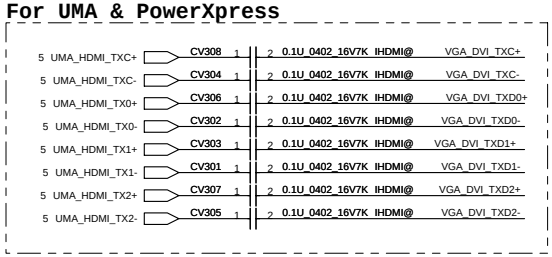
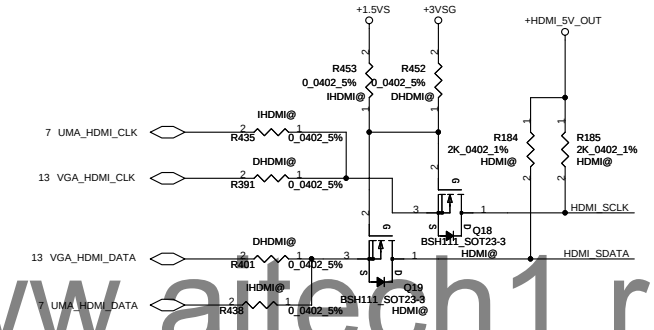
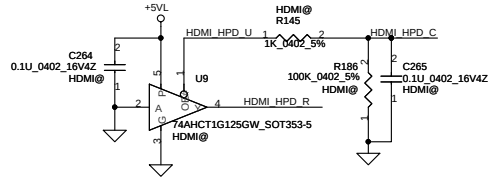
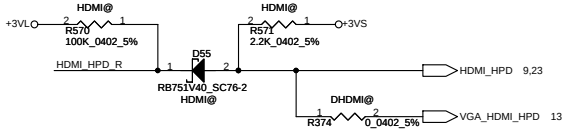
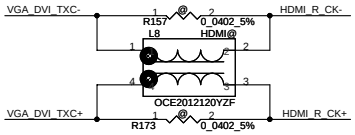
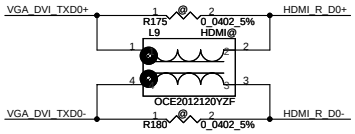


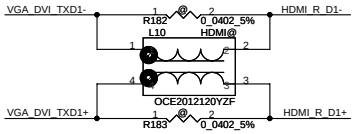


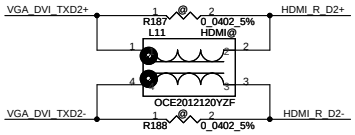


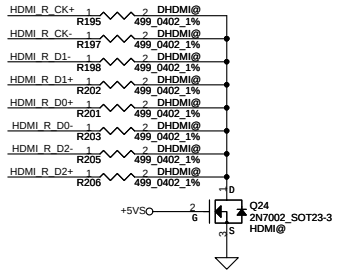


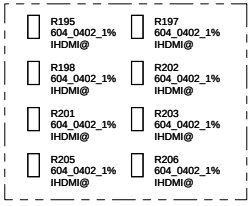


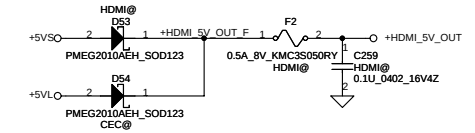




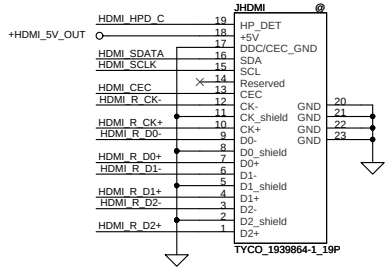








## HDMI Connector



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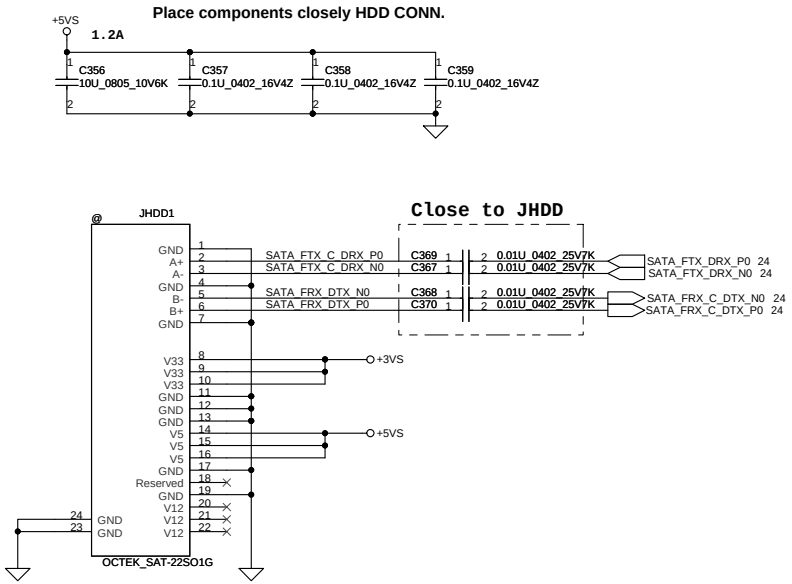
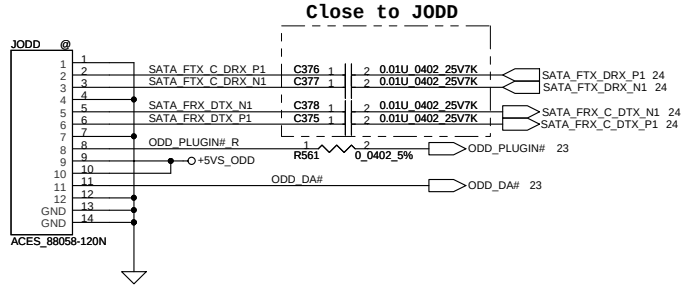
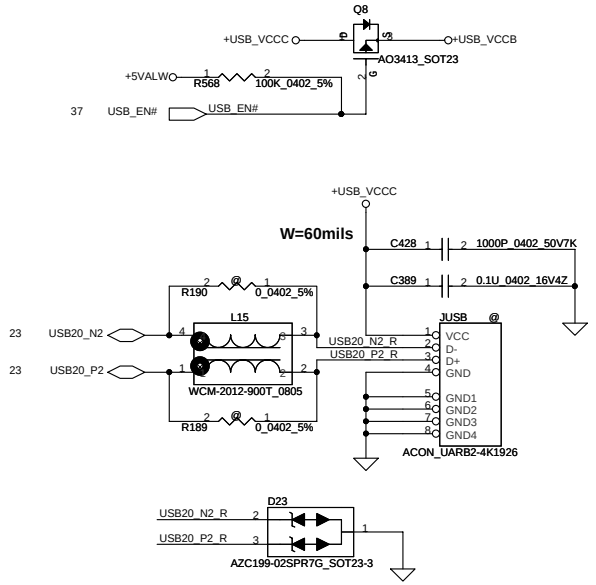
## SATA HDD Conn.




## SATA ODD Conn.




## USB Board@ Left Side

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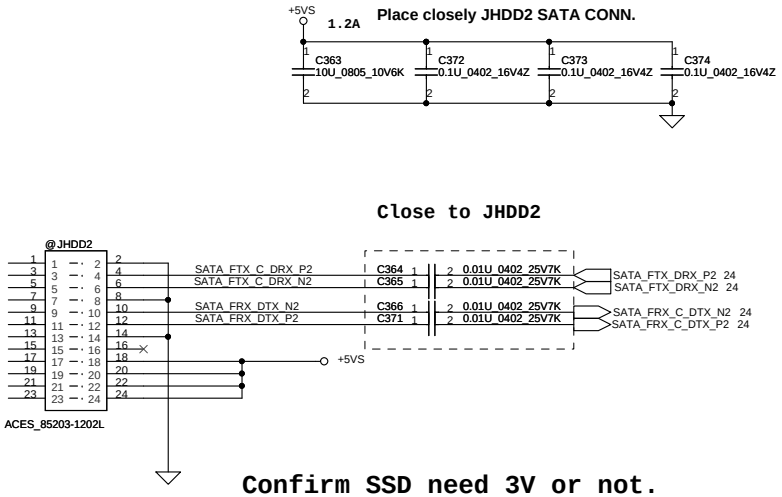
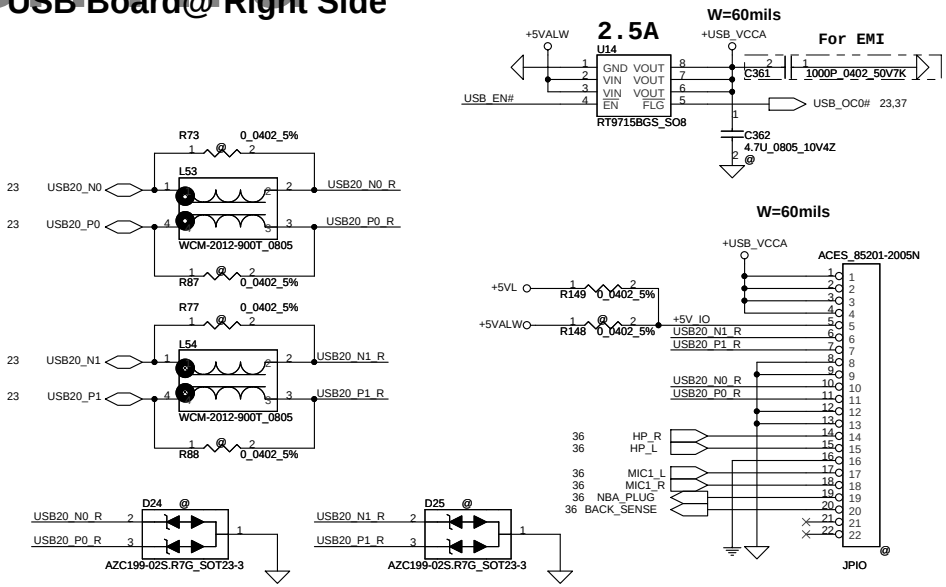
## SATA 2nd HDD Conn.




**Confirm SSD need 3V or not.**

## USB Board@ Right Side

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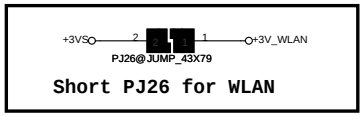
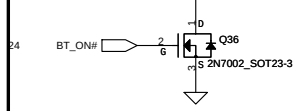
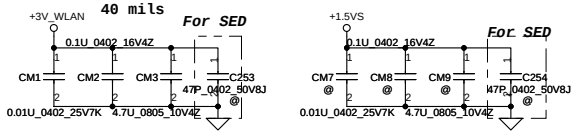
## Slot 1 Half PCIe Mini Card-WLAN

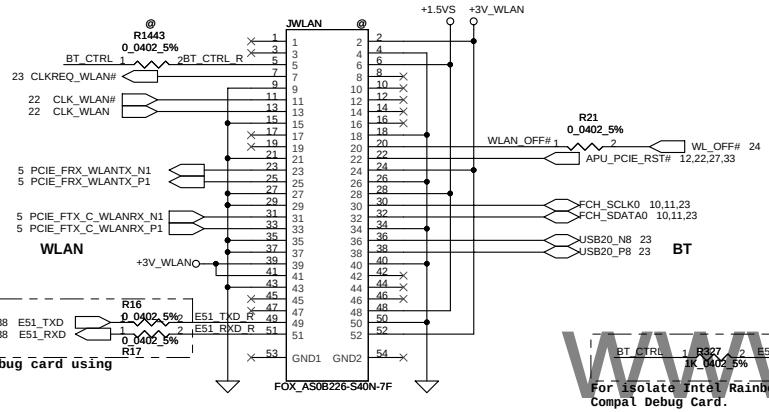


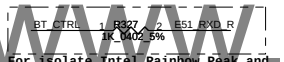

**WLAN&BT Combo module circuits**

| | BT on module Enable | BT on module Disable |
|---|---|---|
| BT_CRTL | H | L |
| BT_ON# | L | H |



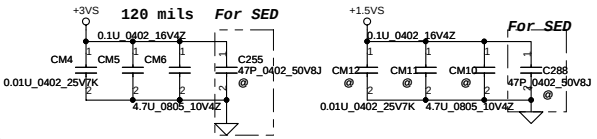



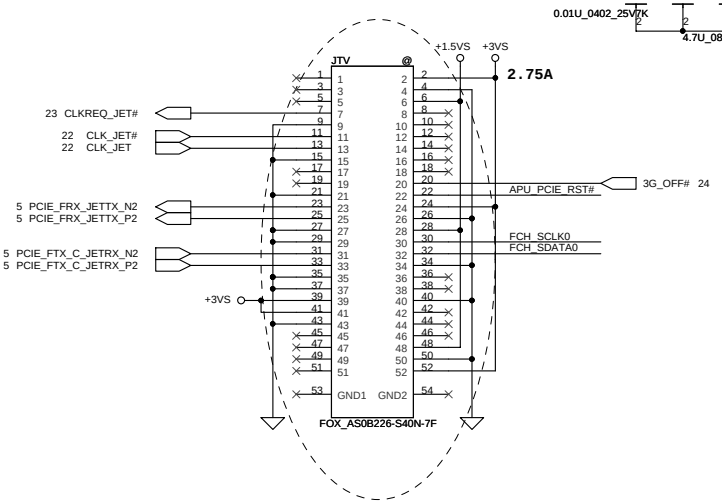




For isolate Intel Rainbow Peak and Compal Debug Card.

## Slot 2 Half PCIe Mini Card- JET

Remove 3G/TV tuner




Need to double check JET pin define

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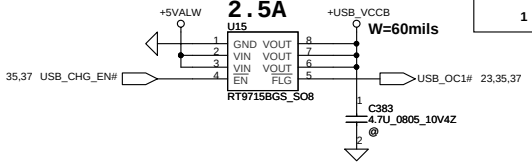
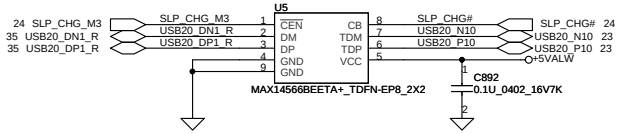
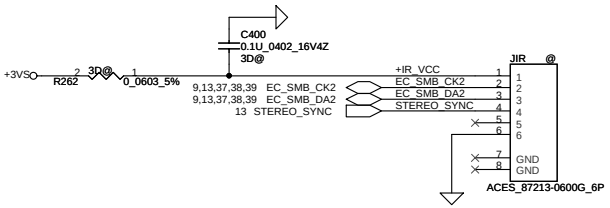
## USB Sleep & Charge:
## Auto-Mode
## Mode3

| MAX14566B | | |
|---|---|---|
| CB SLP_CHG# | CEN# SLP_CHG_M3 | STATUS |
| 0 | 0 | AUTO MODE |
| 0 | 1 | Force Dedicated charger mode (MODE3) |
| 1 | X | Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM |




## IR Emitter Connector

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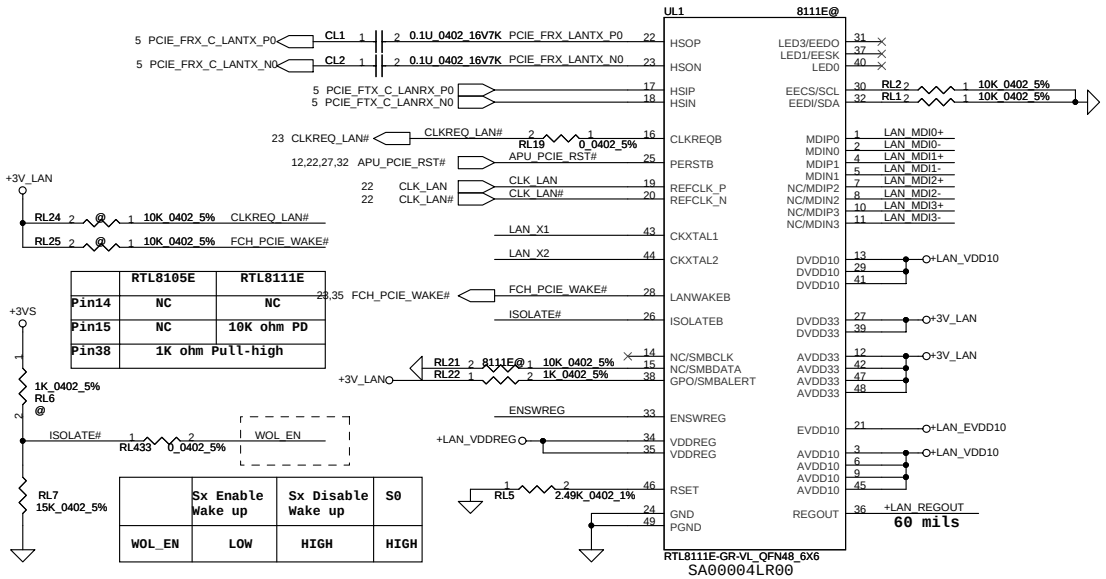


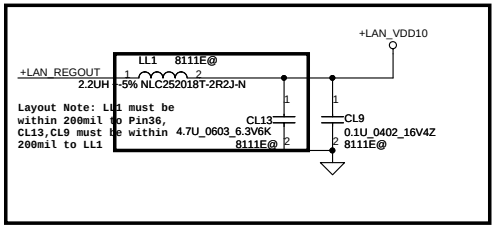


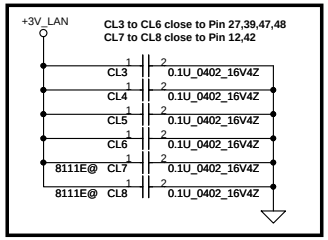


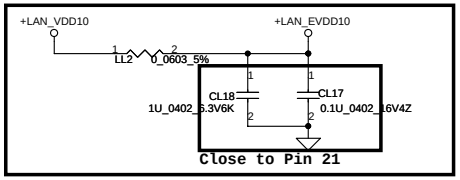


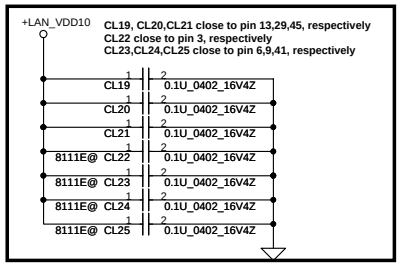


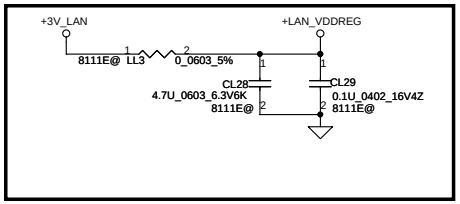


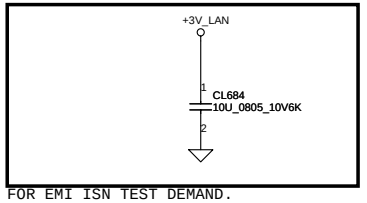


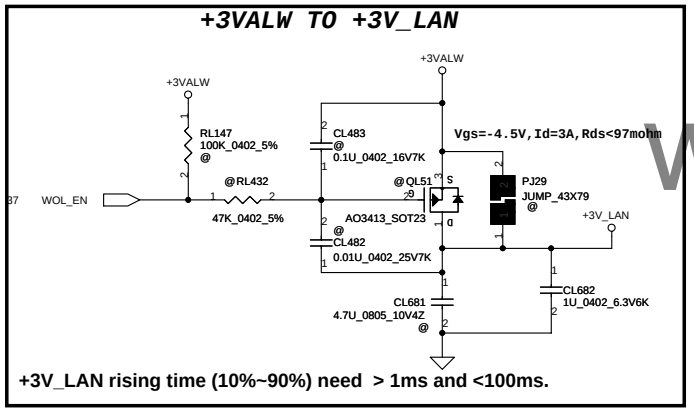


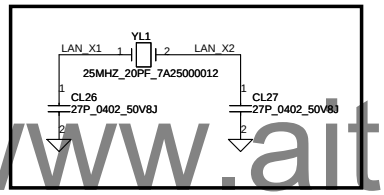


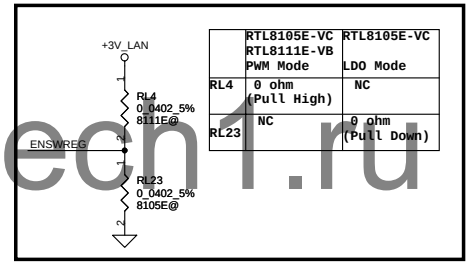


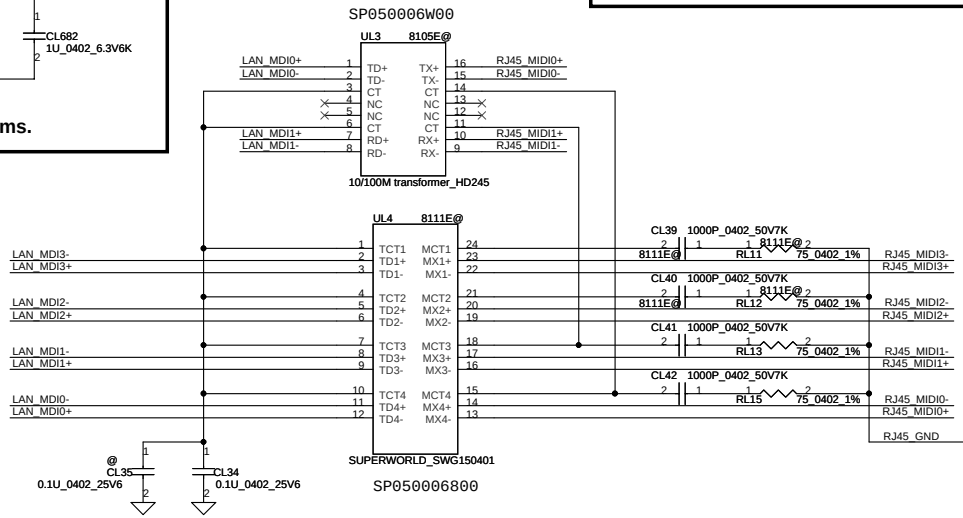


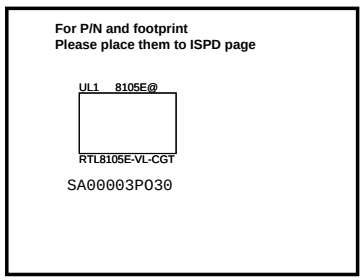


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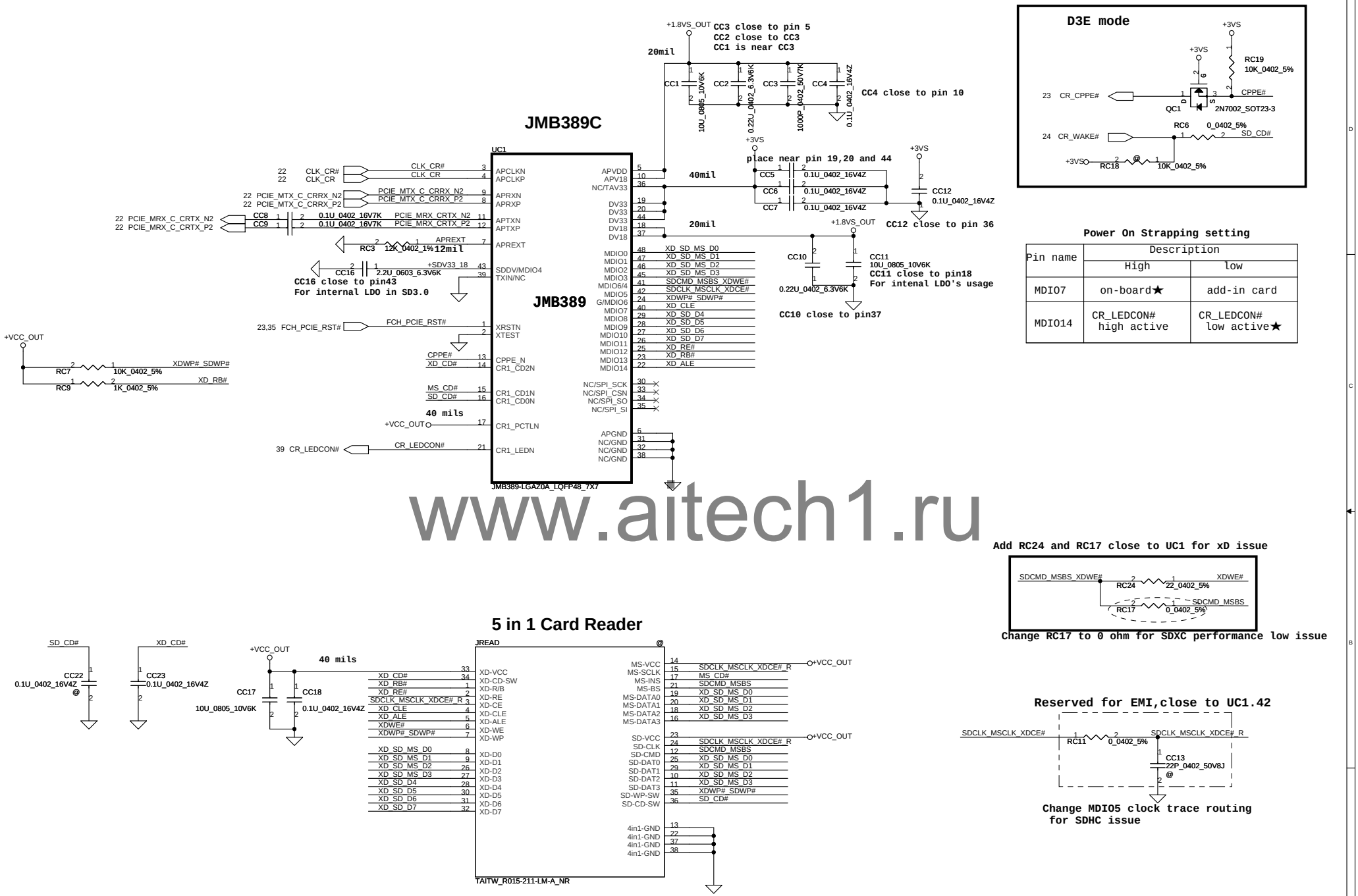


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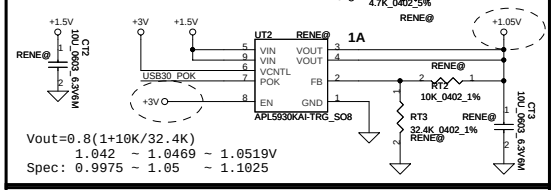
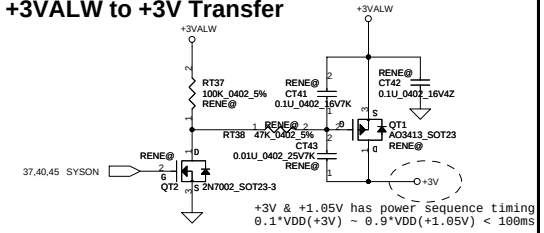
## +1.5V to +1.05V Transfer

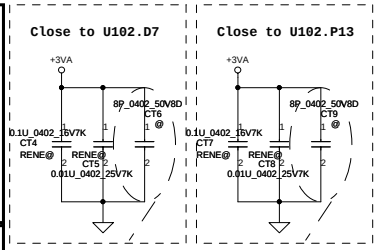



Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

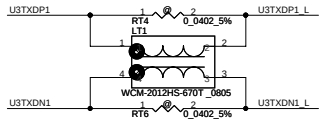
## +3VALW to +3V Transfer




+3V & +1.05V has power sequence timing
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms




Follow Vendor recommend.

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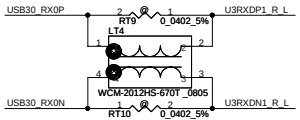


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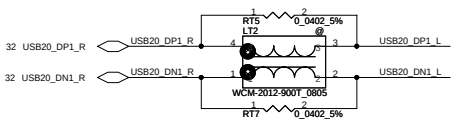
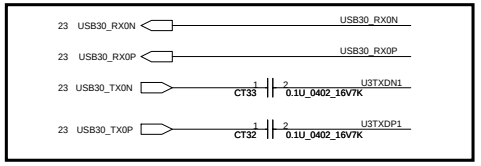
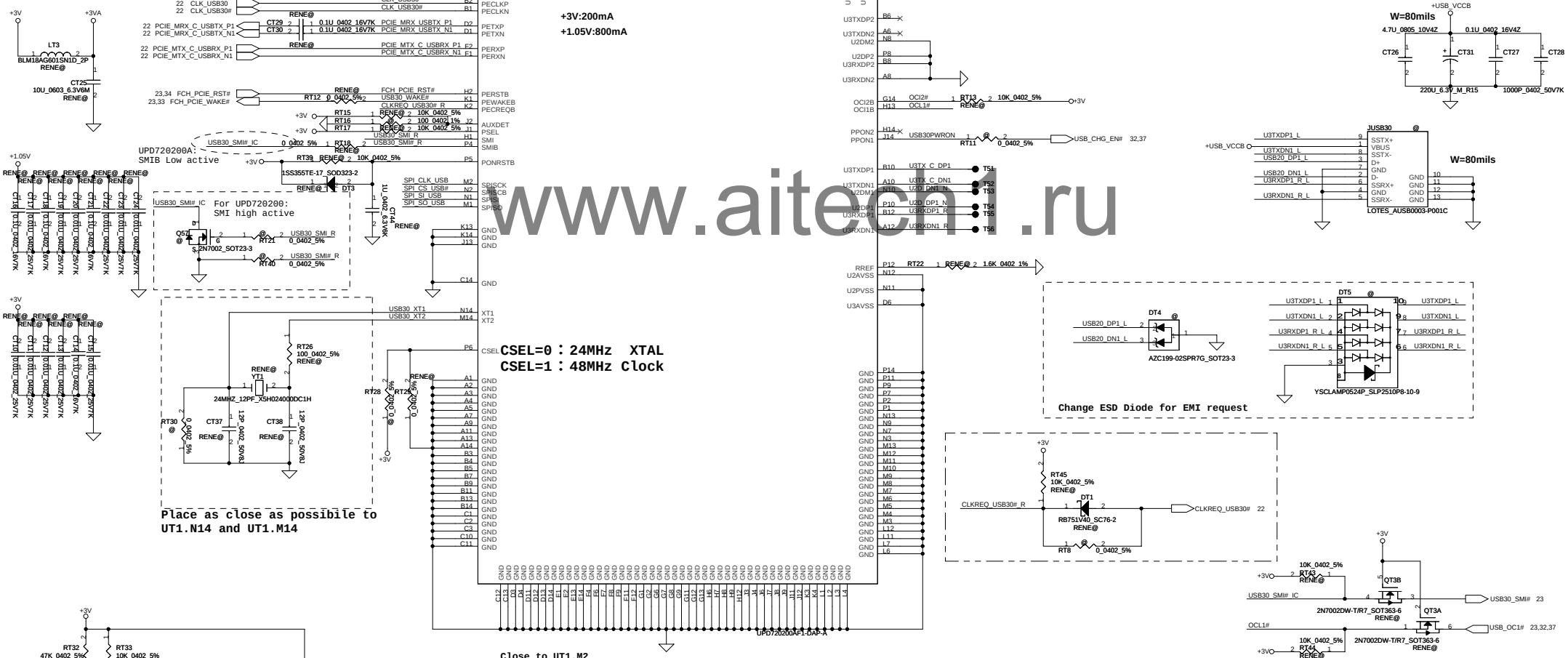
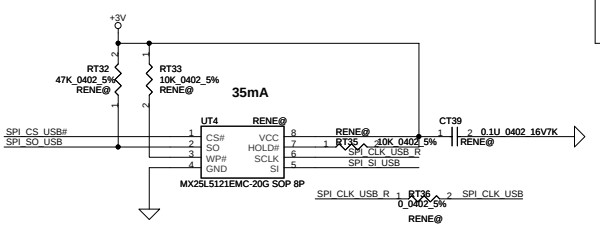


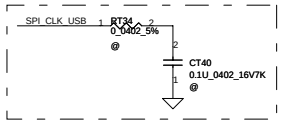

SM070000K00

**Co-Layout with Hudson M3 internal USB3.0**
**Place co-layout resistors close to UT1**







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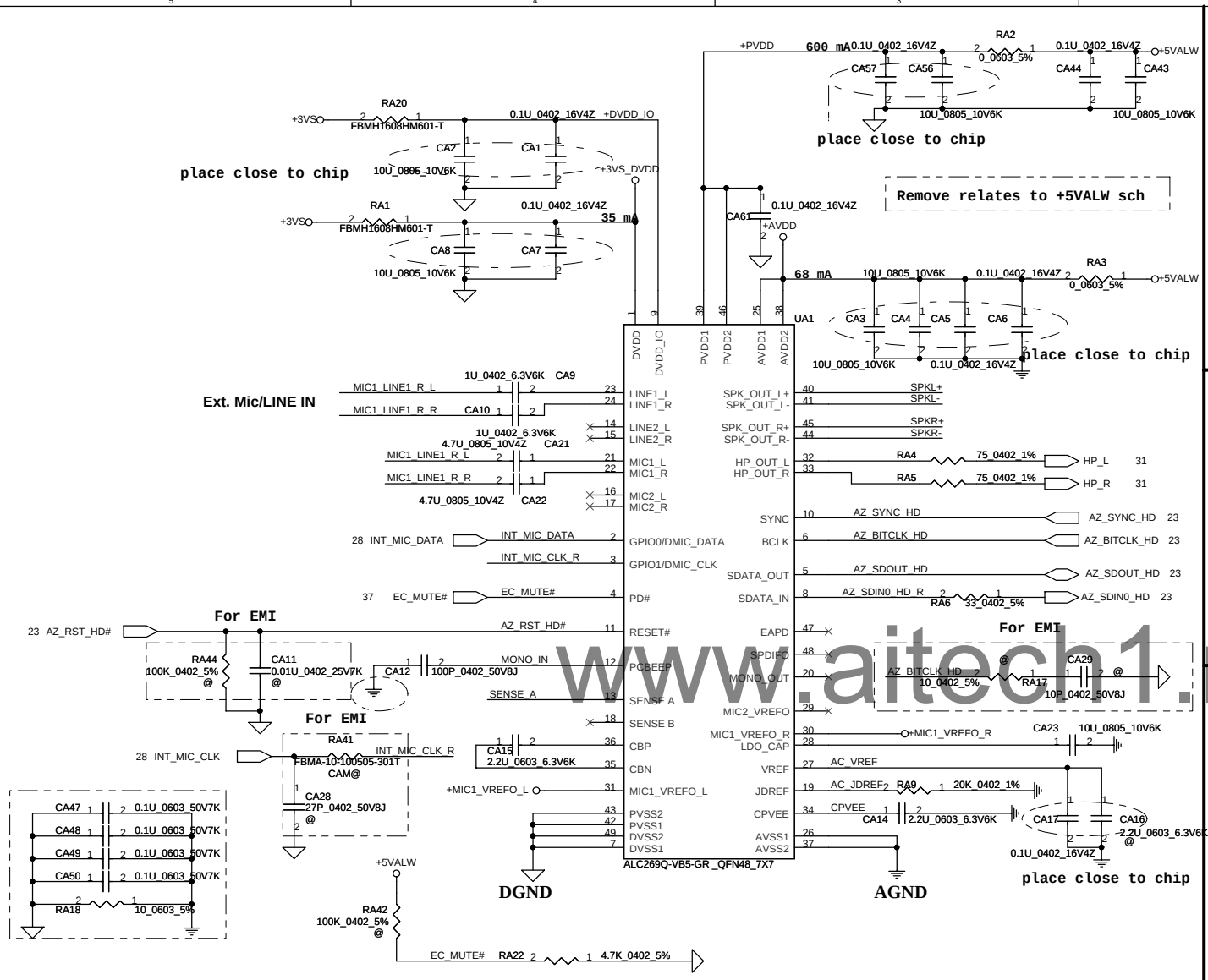
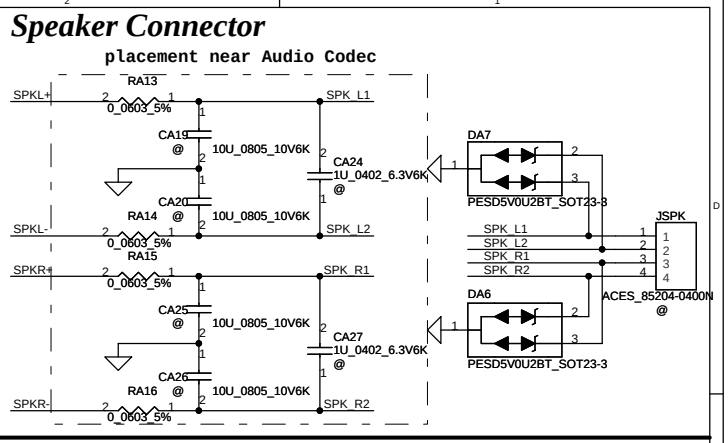
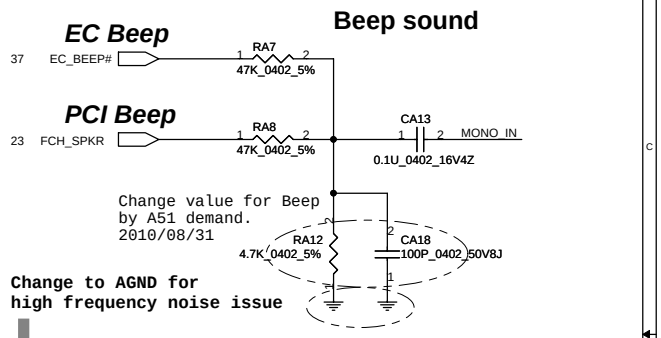
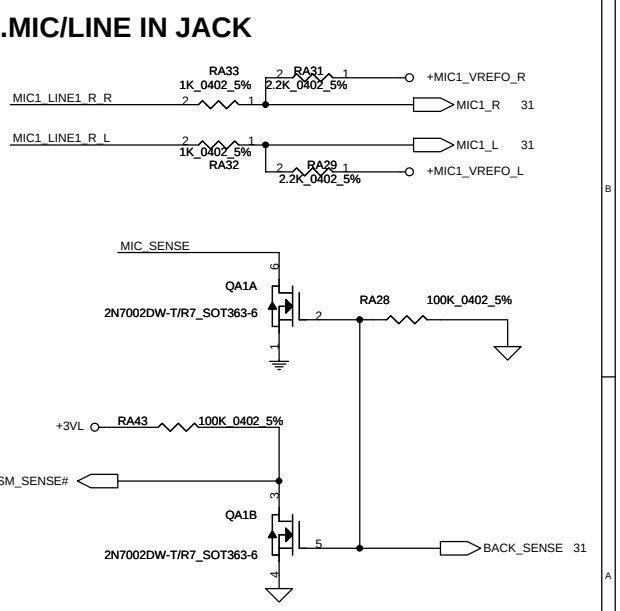
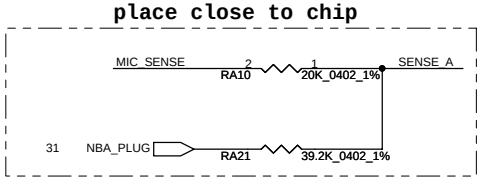



| Sense Pin | Impedance | Codec Signals | Function |
|---|---|---|---|
| SENSE A | 39.2K | PORT-I (PIN 32, 33) | Headphone out |
| | 20K | PORT-B (PIN 21, 22) | Ext. MIC |
| | 10K | PORT-C (PIN 23, 24) | |
| | 5.1K | (PIN 48) | |
| SENSE B | 39.2K | PORT-E (PIN 14, 15) | |
| | 20K | PORT-F (PIN 16, 17) | |
| | 10K | PORT-H (PIN 20) | |

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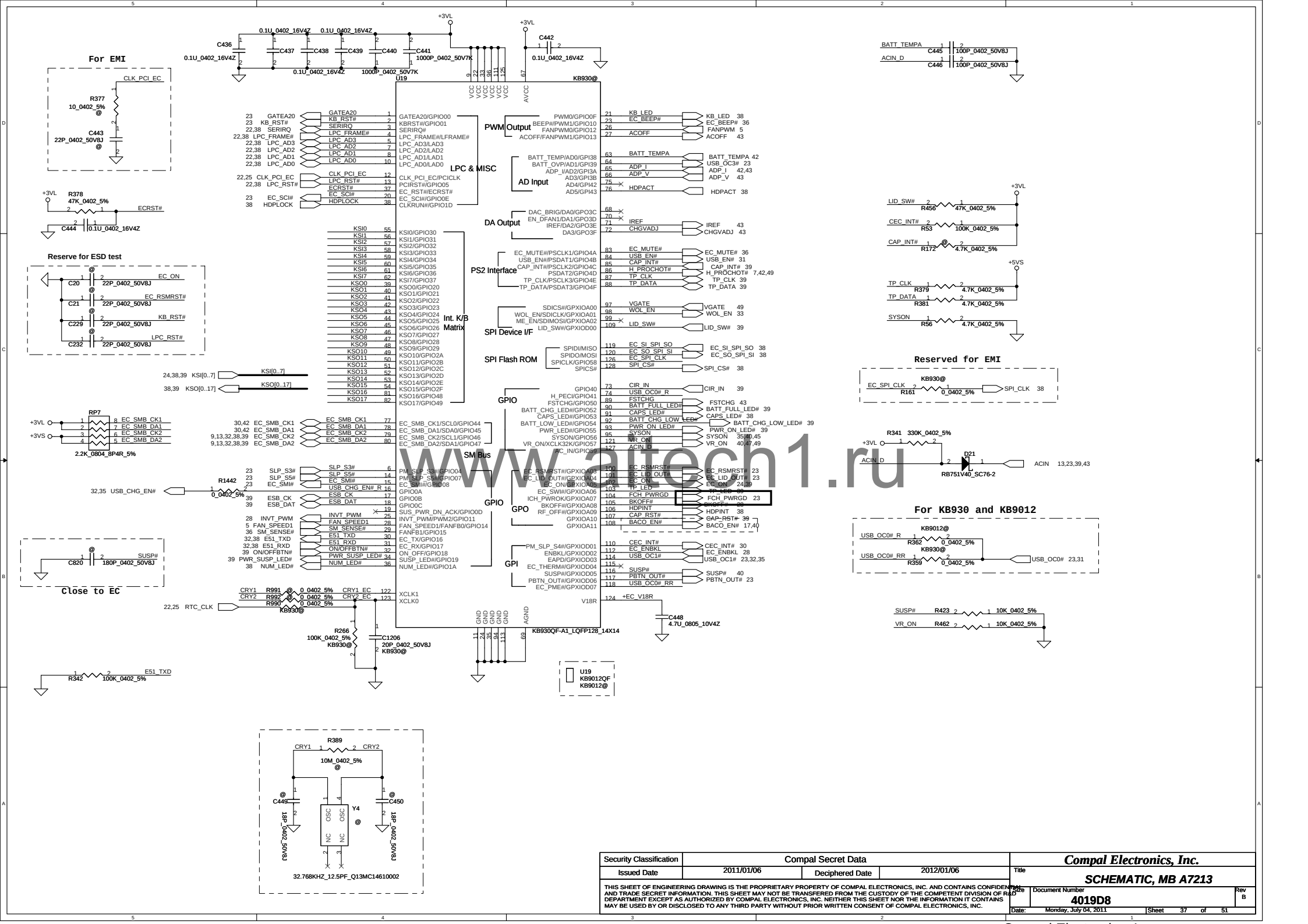


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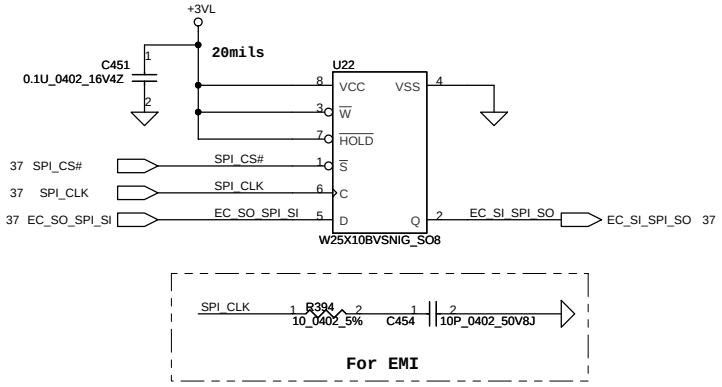
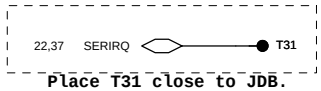
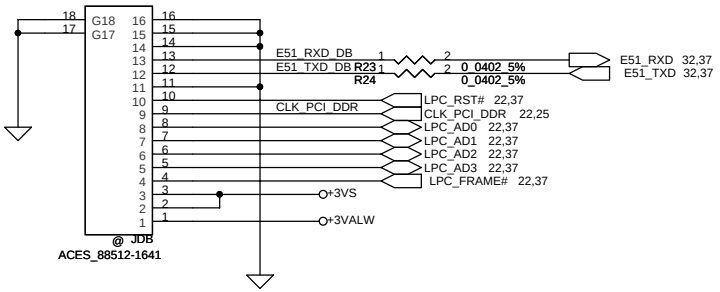
# SPI Flash (128KB)



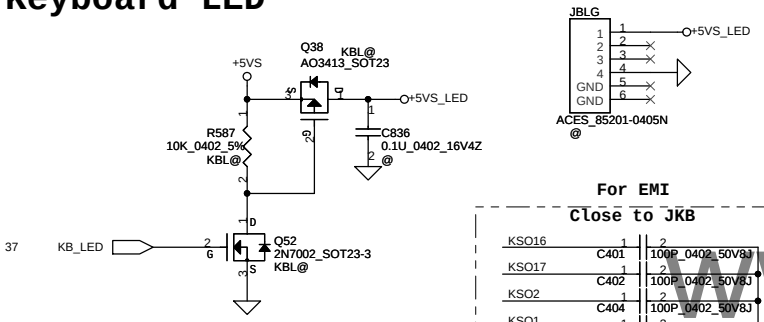

# LPC Debug Port

Place JDB under DDR DIMM.

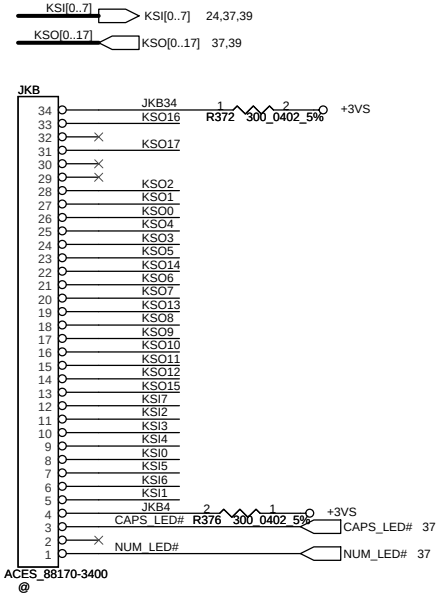


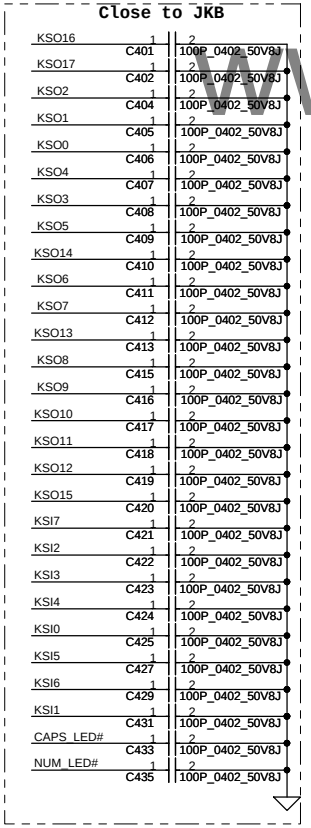

# Keyboard LED



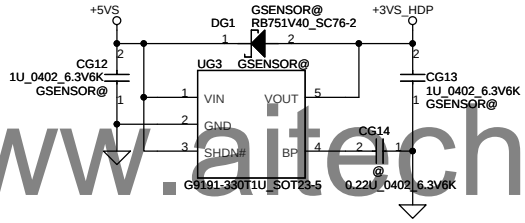

# KEYBOARD CONN.



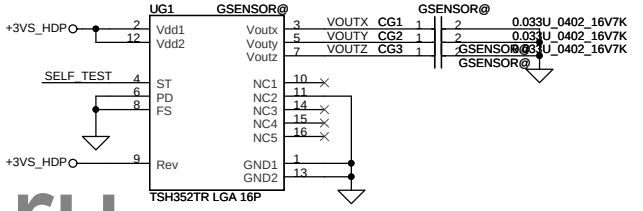

## For EMI Close to JKB

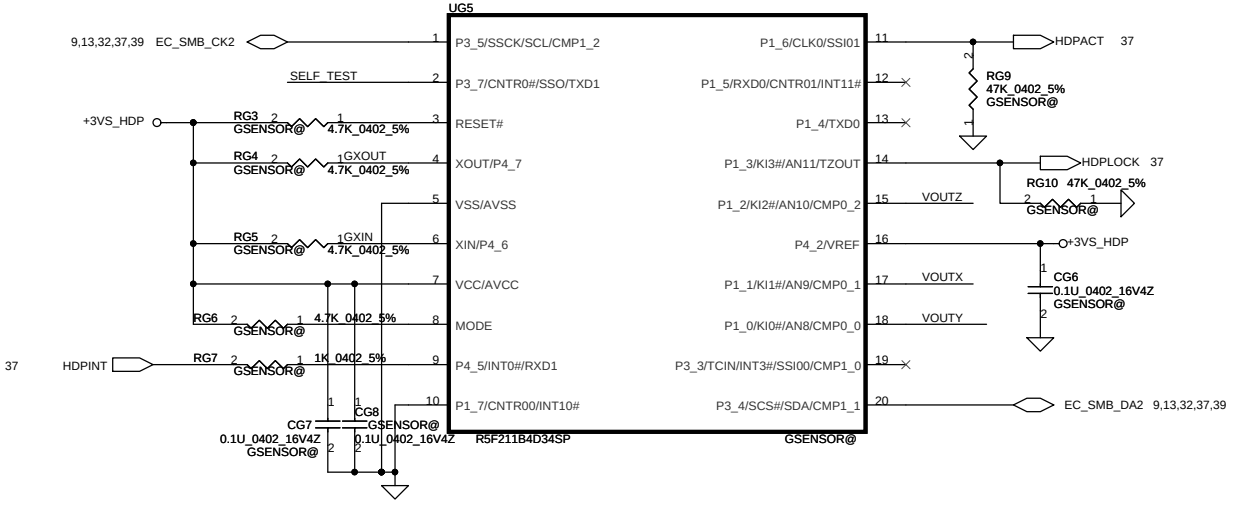



# G-Sensor




## Place UG1 on TOP Layer

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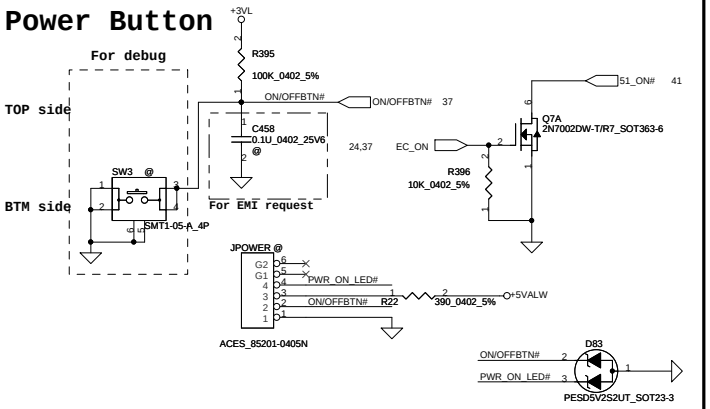
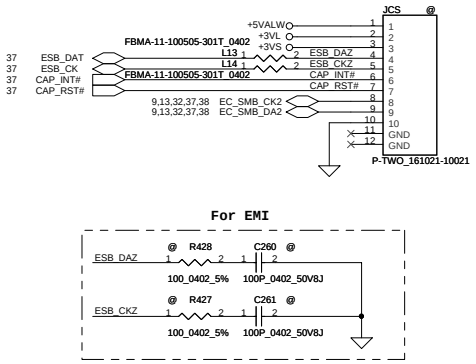
## Power Button



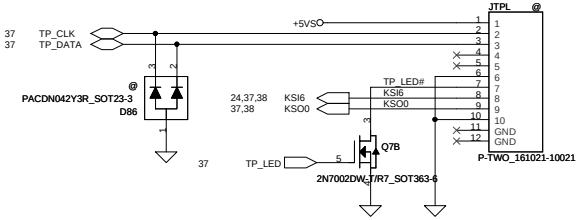

## Caps Sensor/Light Sensor Conn.



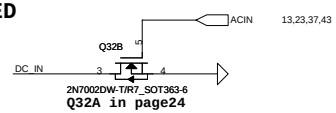

### For EMI



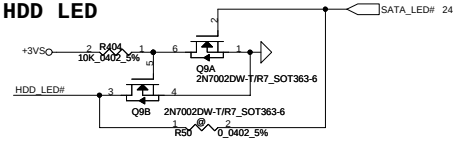

## Touchpad & Light Pipe Connector



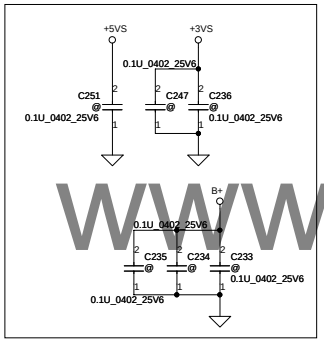

## DC-IN LED

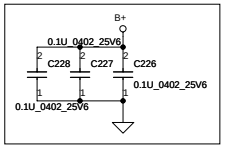



## HDD LED



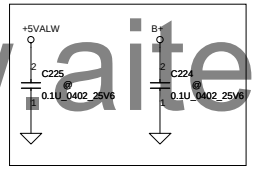

Reserve for ESD request



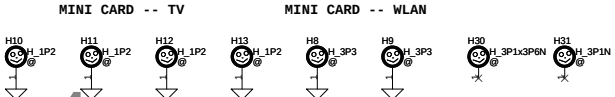

Reserve for EMI request

Close to H17




Reserve for ESD request

## Screw Hole

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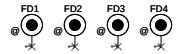
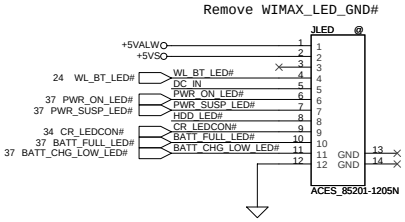
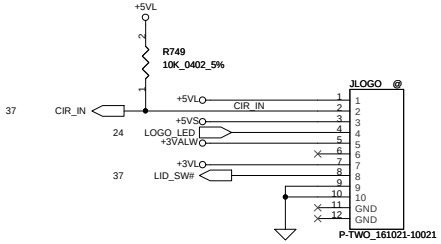



## LED/B Connector




## LOGO/B Connector




## ISPD

WHPRORR3@
SA00004C790

UV1 WHPRORR1@
SA00004C780
216-0810005 A11 WHISTLER PRO

ZZZ
DAZ0K600100
PCB LA-7213P

U1 HUDM3R1@
SA000043I60
218-0755022 A13 HUDSON-M3

PJP1 45@
DC30100AA00
PJP1

HUDM3R3@
SA000043I70

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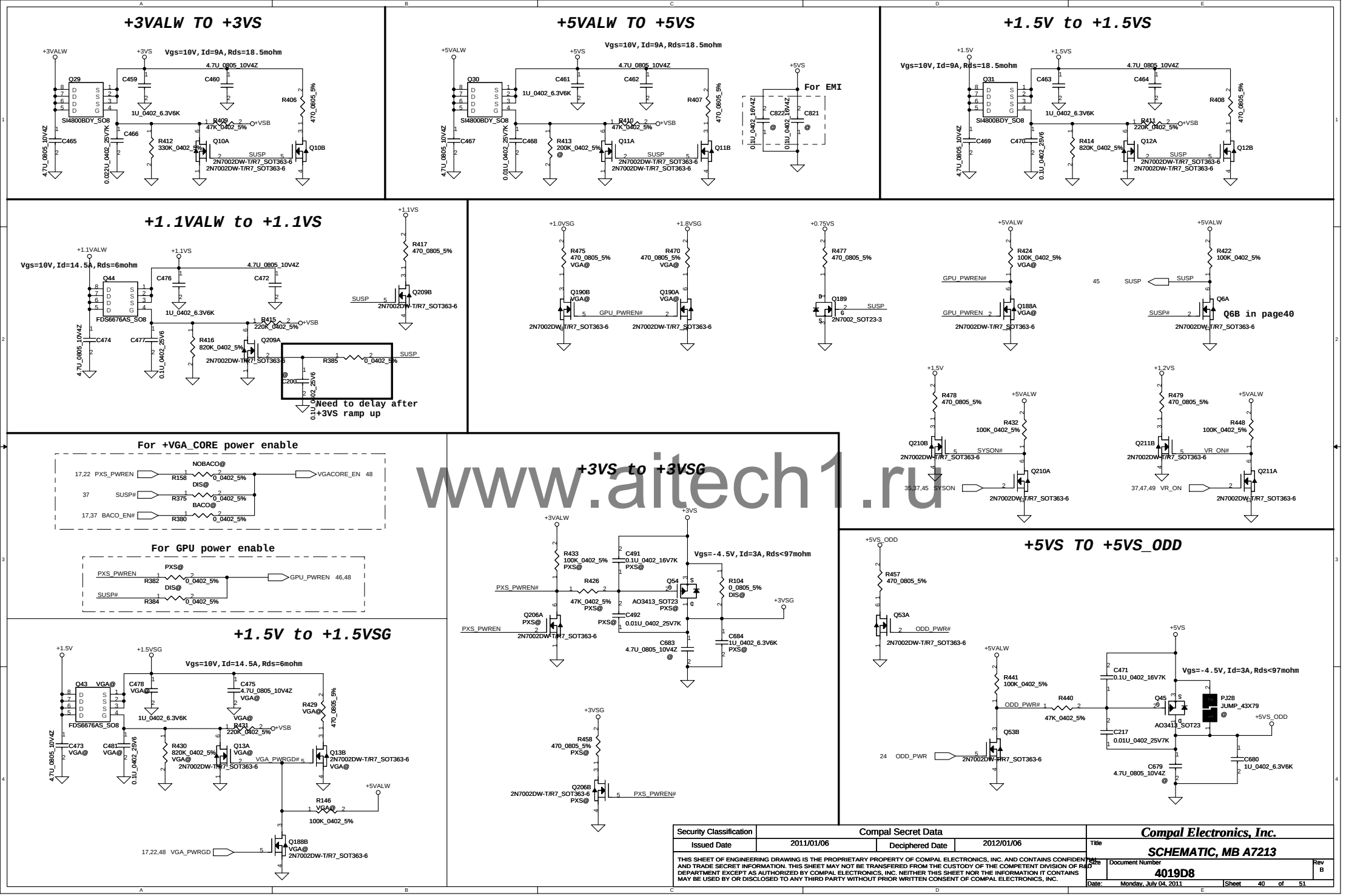


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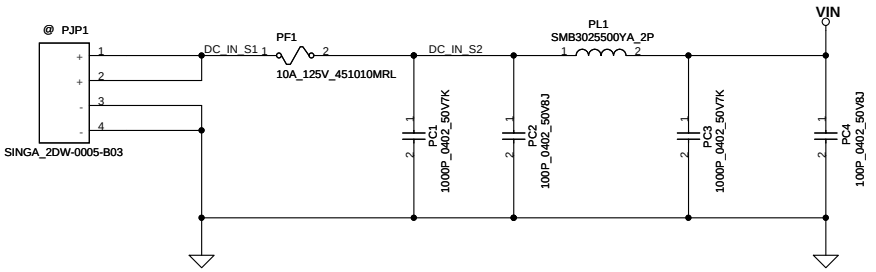


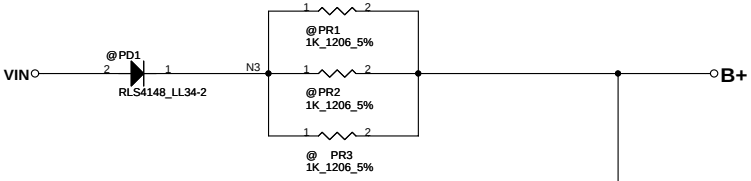


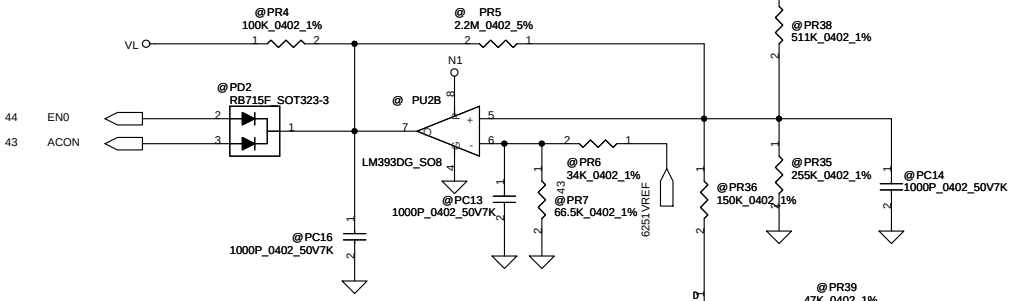


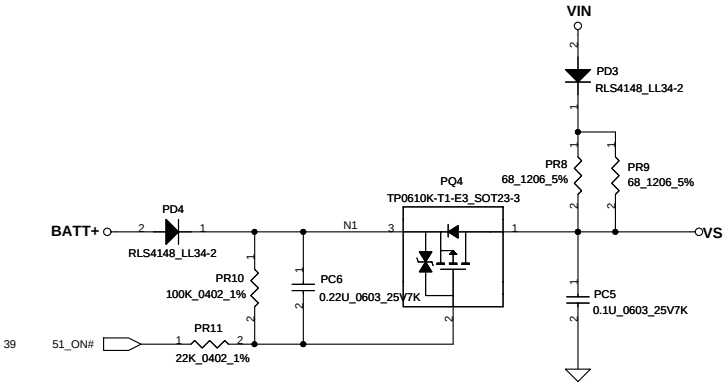


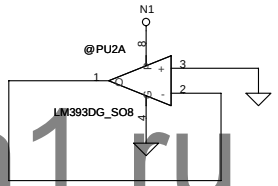


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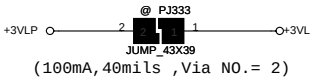
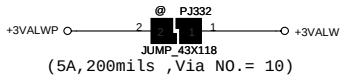
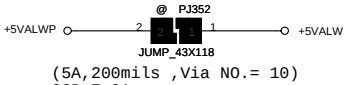



(100mA,40mils ,Via NO.= 2)




(5A,200mils ,Via NO.= 10)
OCP=7.7A

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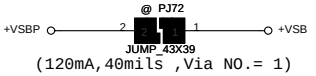
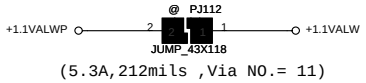
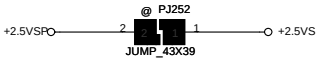
OCP=7.9A

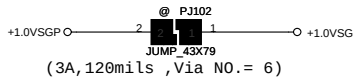



(120mA,40mils ,Via NO.= 1)

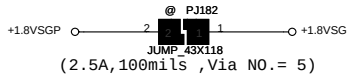



(5.3A,212mils ,Via NO.= 11)
OCP=6.81A

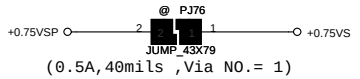


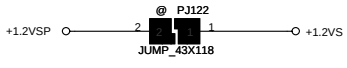

(3A,120mils ,Via NO.= 6)



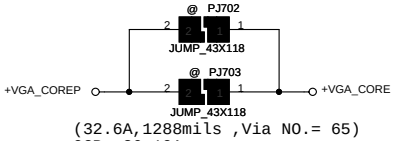

(2.5A,100mils ,Via NO.= 5)



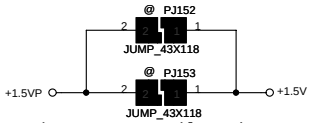

(0.5A,40mils ,Via NO.= 1)




(6.5A,260mils ,Via NO.= 13)
OCP=8.55A

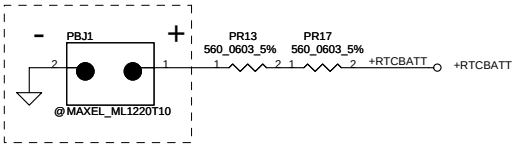



(32.6A,1288mils ,Via NO.= 65)
OCP= 36.19A




(DIS 20A, 800mils ,Via NO.= 40,
OCP=24.13A)
(UMA 8.5A, OCP=10.44A)

## RTC Battery




**SP093MX0000**

**ACIN**

| Precharge detector | Min. | typ. | Max |
|---|---|---|---|
| H-->L | 14.42V | 14.74V | 15.23V |
| L-->H | 15.39V | 15.88V | 16.39V |

| | | | |
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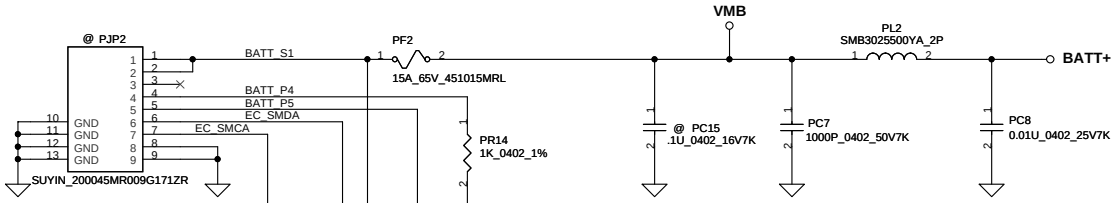
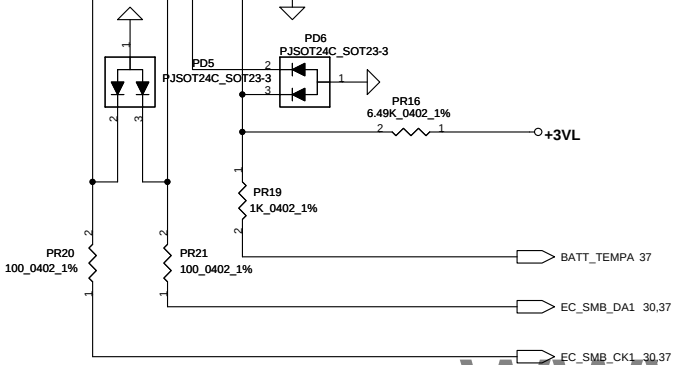
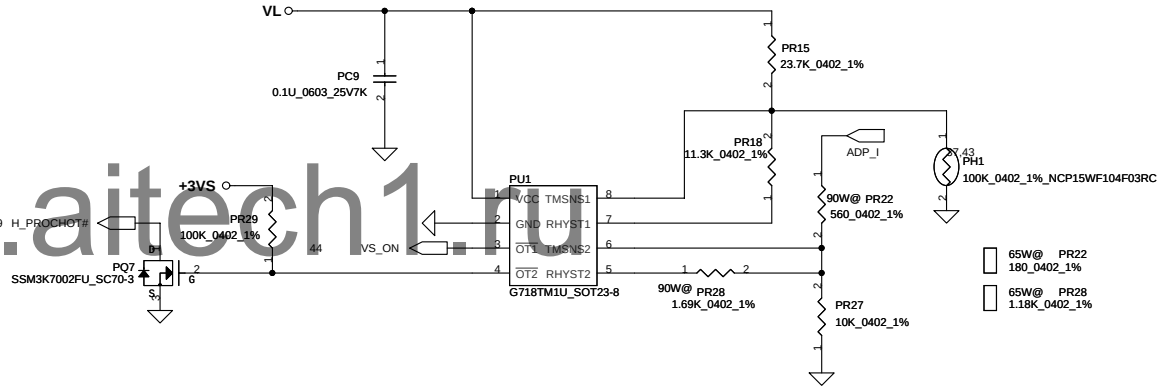


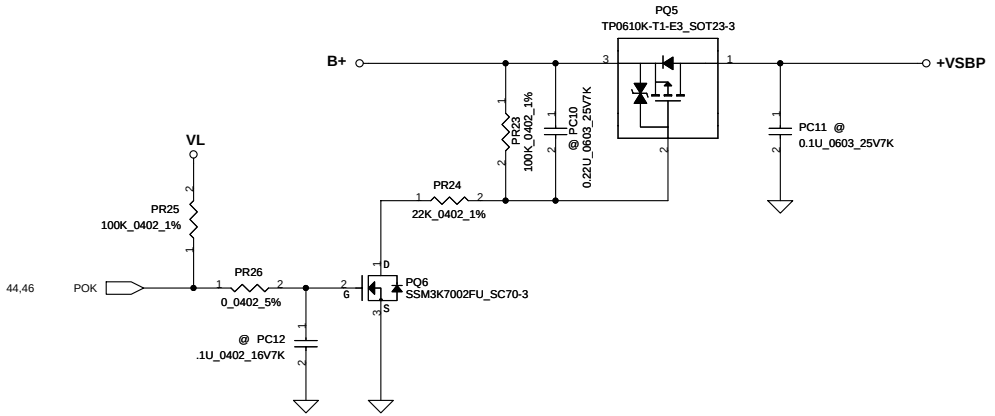




**PH1 under CPU botten side :**
CPU thermal protection at 90 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
Rset = 3 * 7.87K = 23.61K ==> 23.7K
Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K




| Adaptor protection | | | | |
|---|---|---|---|---|
| Adaptor | Throttling point | ADP_I | Recovery point | ADP_I |
| 90W | 113.5W | 1.783V | 86.4W | 1.357V |
| 65W | 71.8W | 1.5V | 62.44W | 1.3V |

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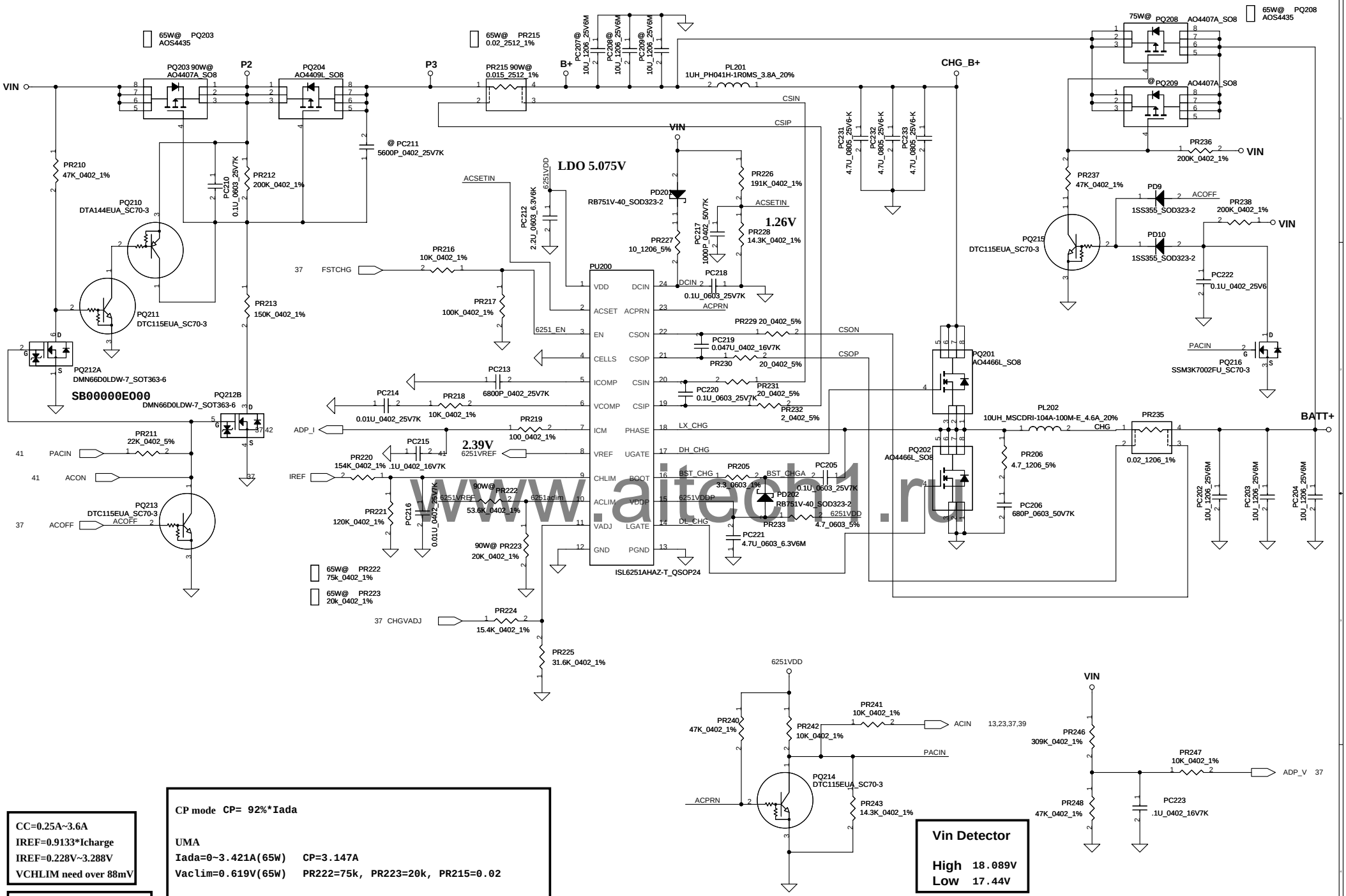


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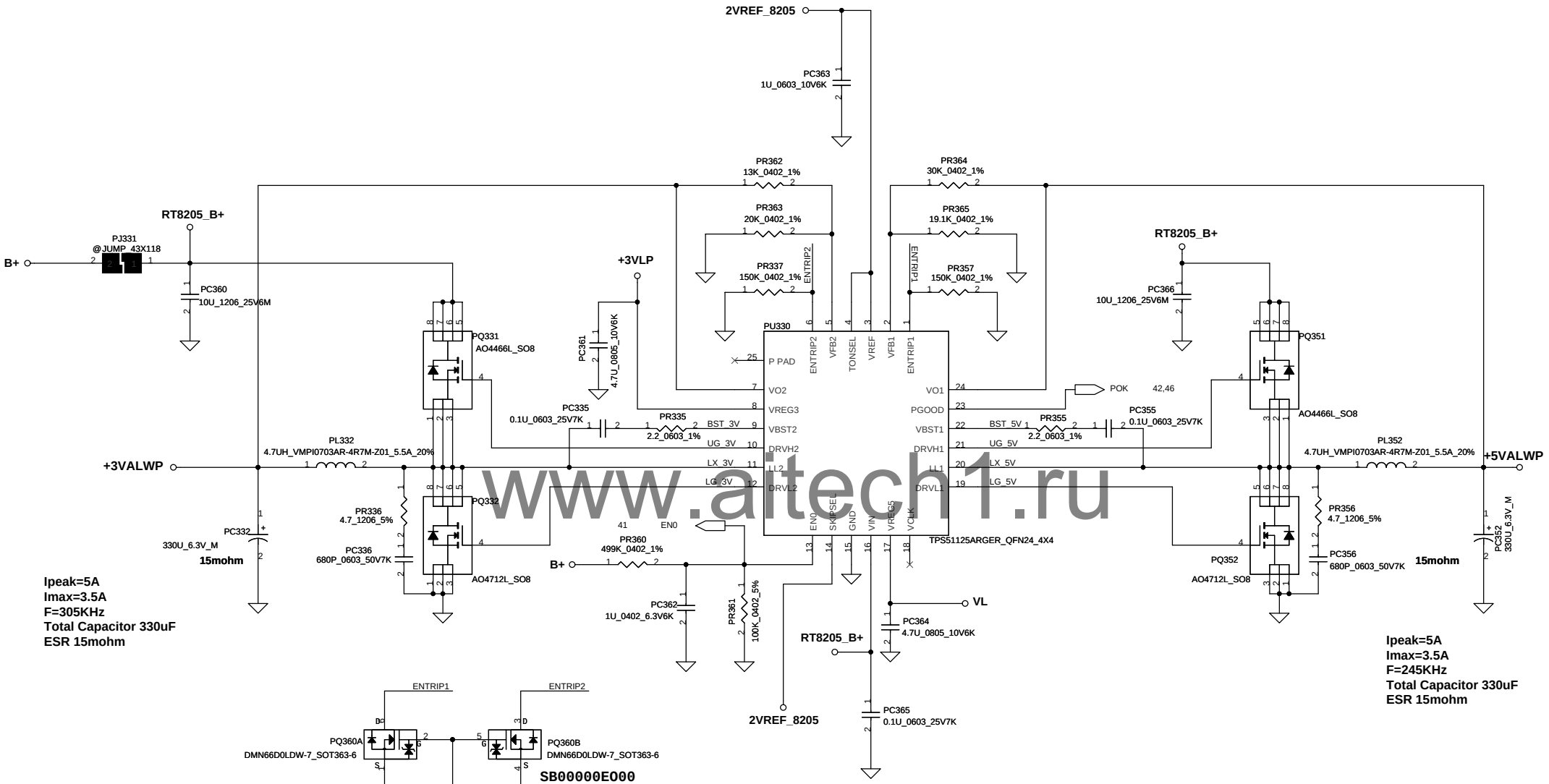


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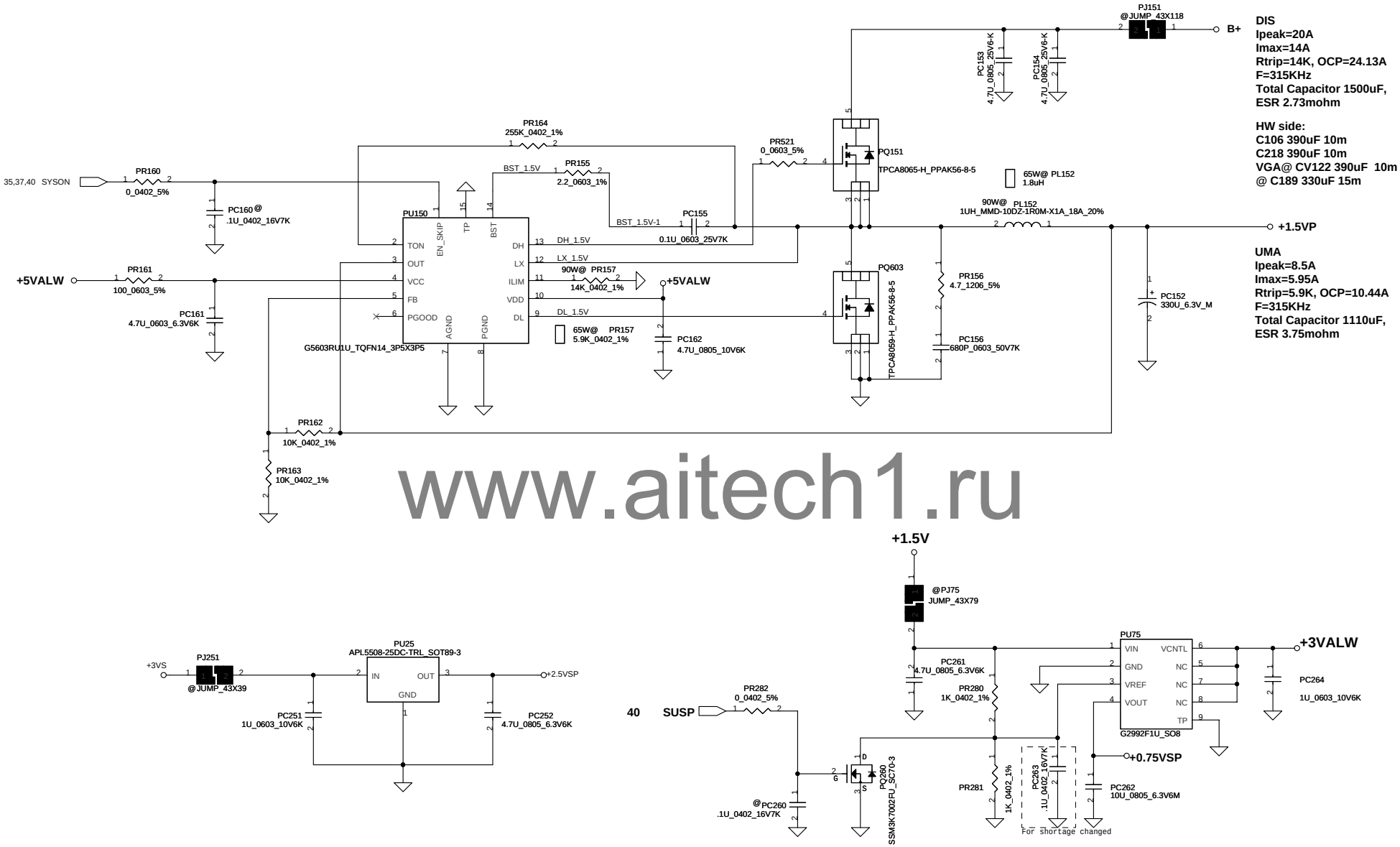


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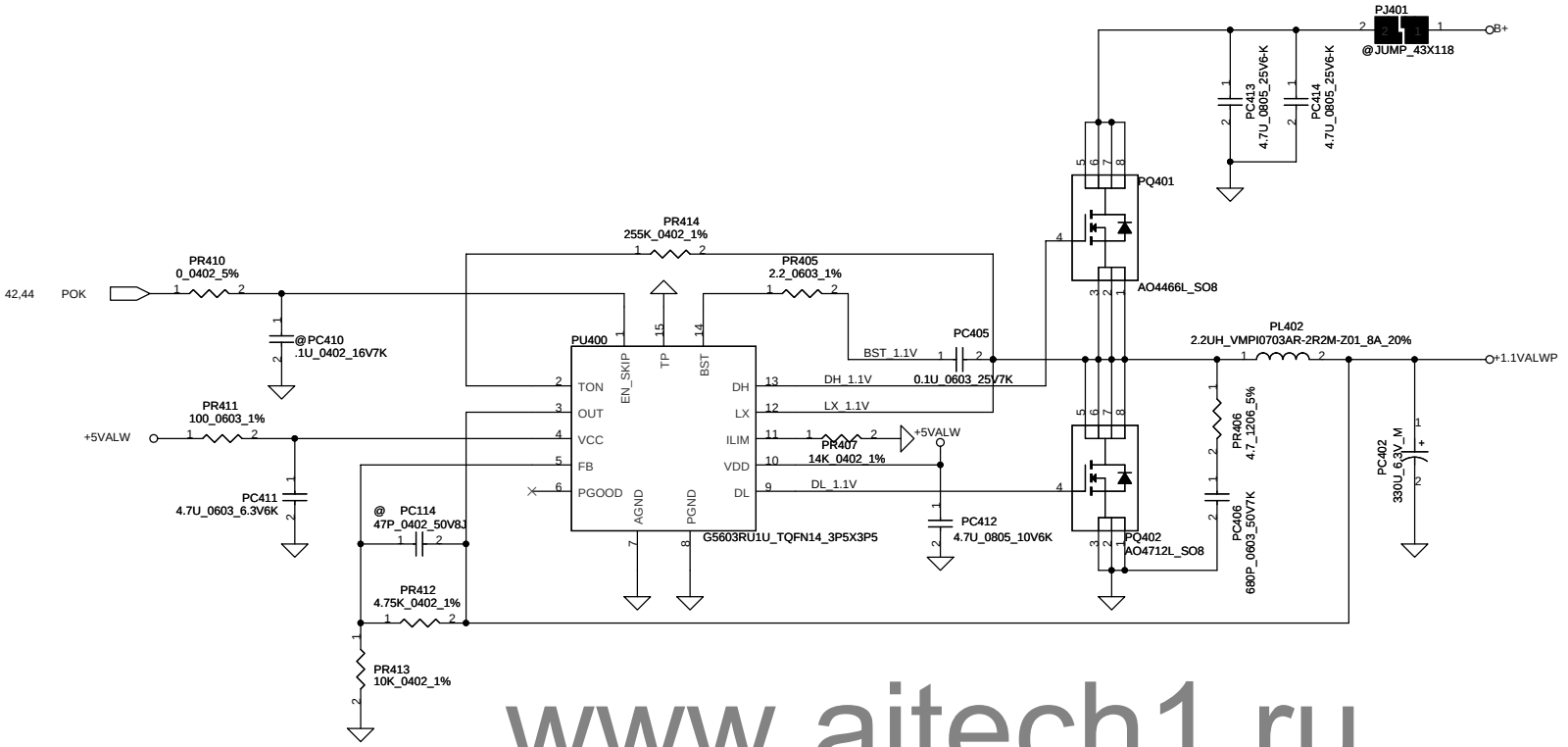


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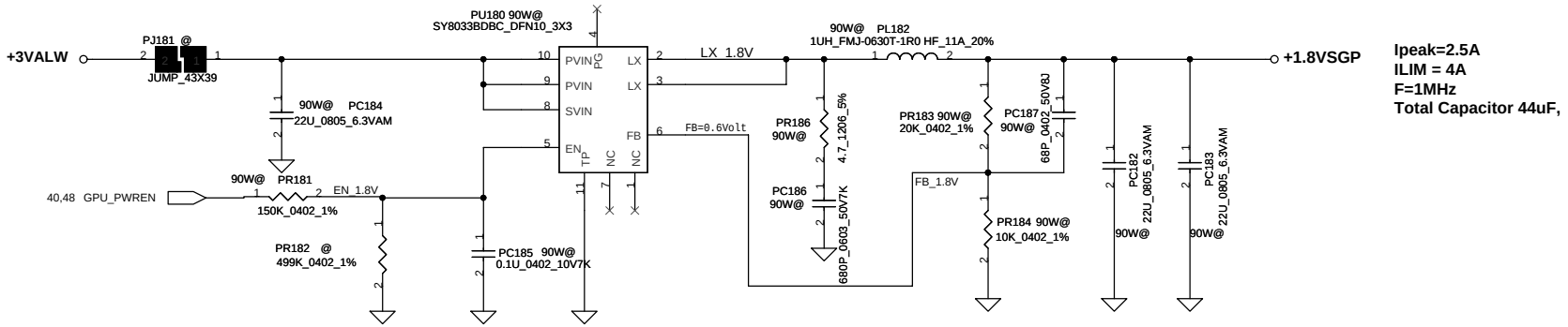


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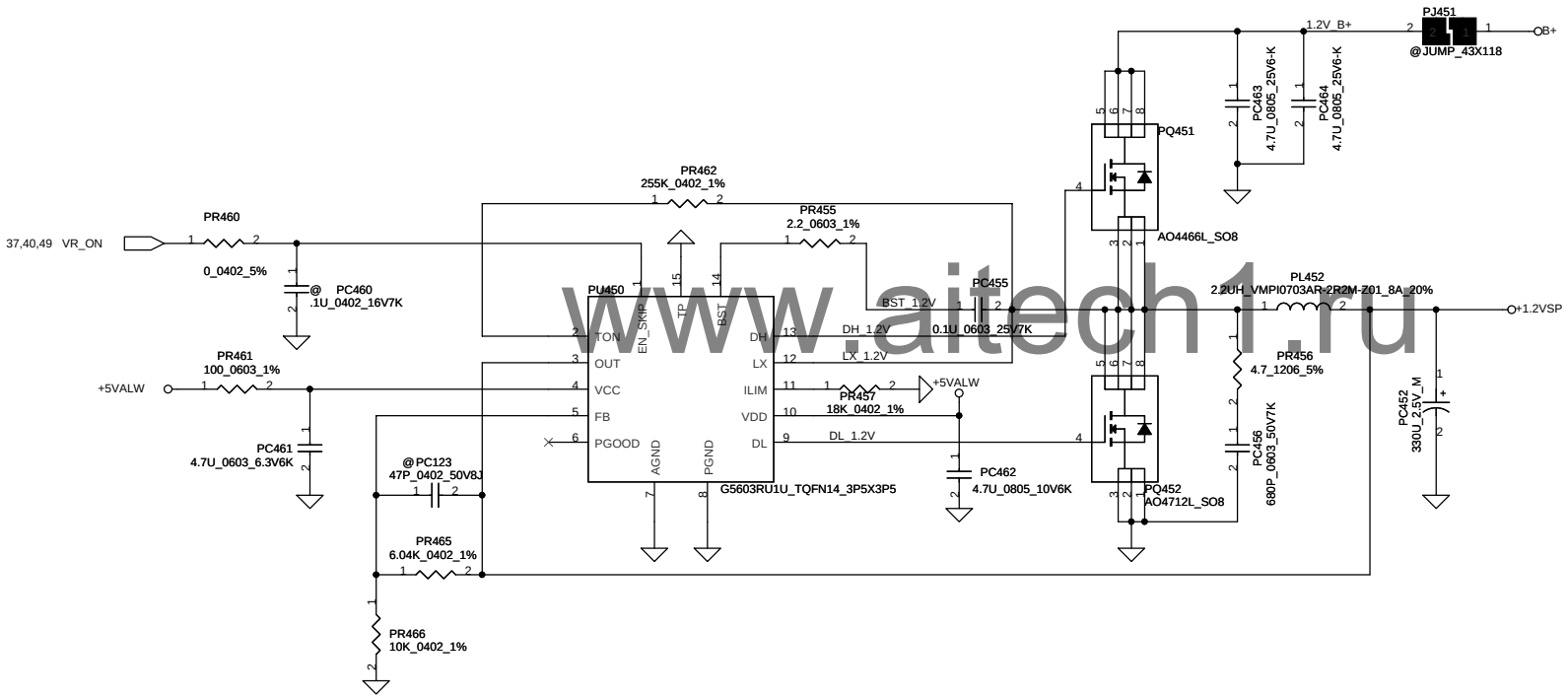


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**Ipeak=6.5A**
**Imax=4.55A**
**Rtrip=18K, OCP=8.37A**
**F=315KHz**
**Total Capacitor 720uF,**
**ESR 6mohm**

**HW side:**
**C130 390uF 10m**

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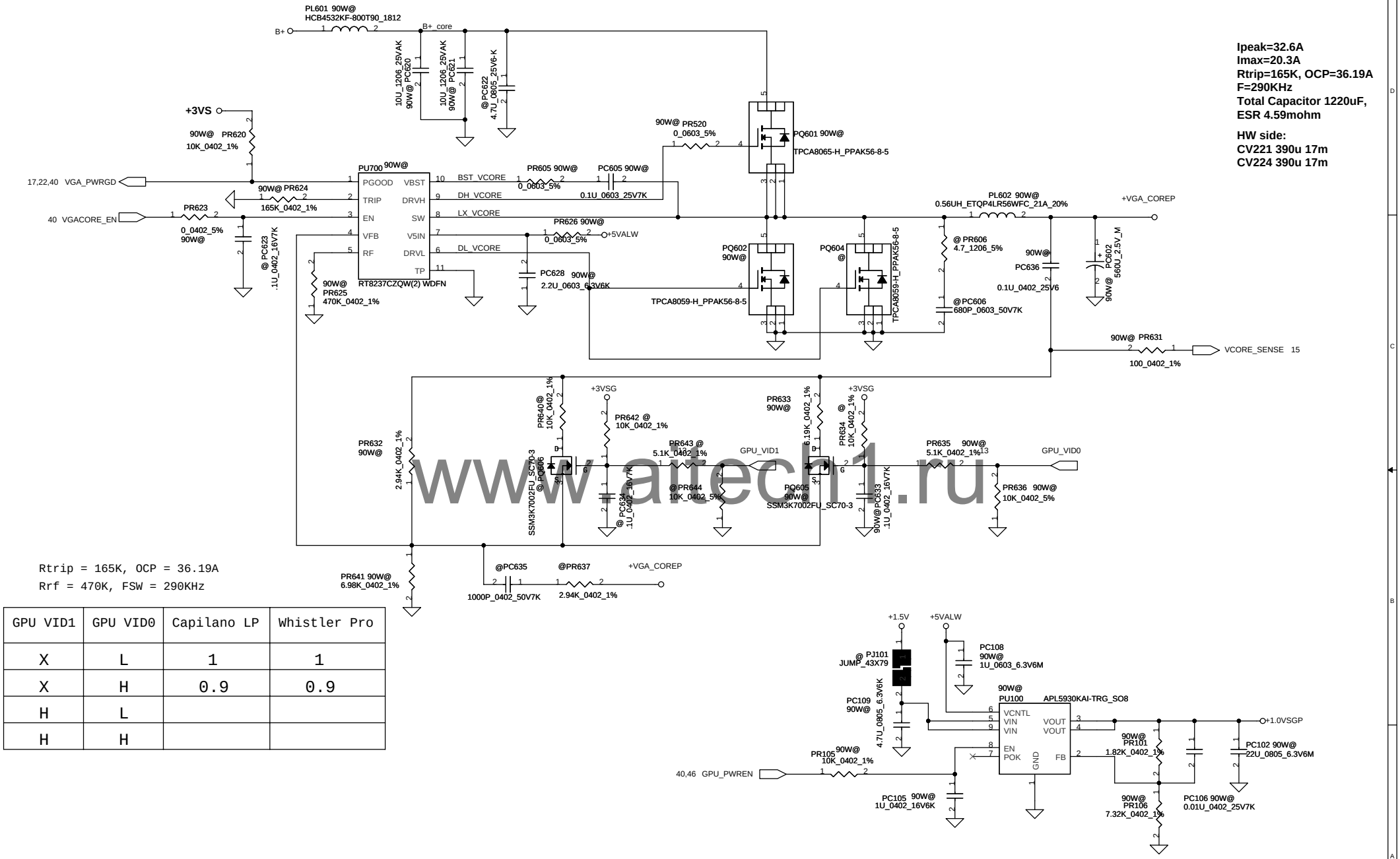


**Ipeak=32.6A**
**Imax=20.3A**
**Rtrip=165K, OCP=36.19A**
**F=290KHz**
**Total Capacitor 1220uF,**
**ESR 4.59mohm**

**HW side:**
**CV221 390u 17m**
**CV224 390u 17m**

Rtrip = 165K, OCP = 36.19A
Rrf = 470K, FSW = 290KHz

| GPU VID1 | GPU VID0 | Capilano LP | Whistler Pro |
|---|---|---|---|
| X | L | 1 | 1 |
| X | H | 0.9 | 0.9 |
| H | L | | |
| H | H | | |

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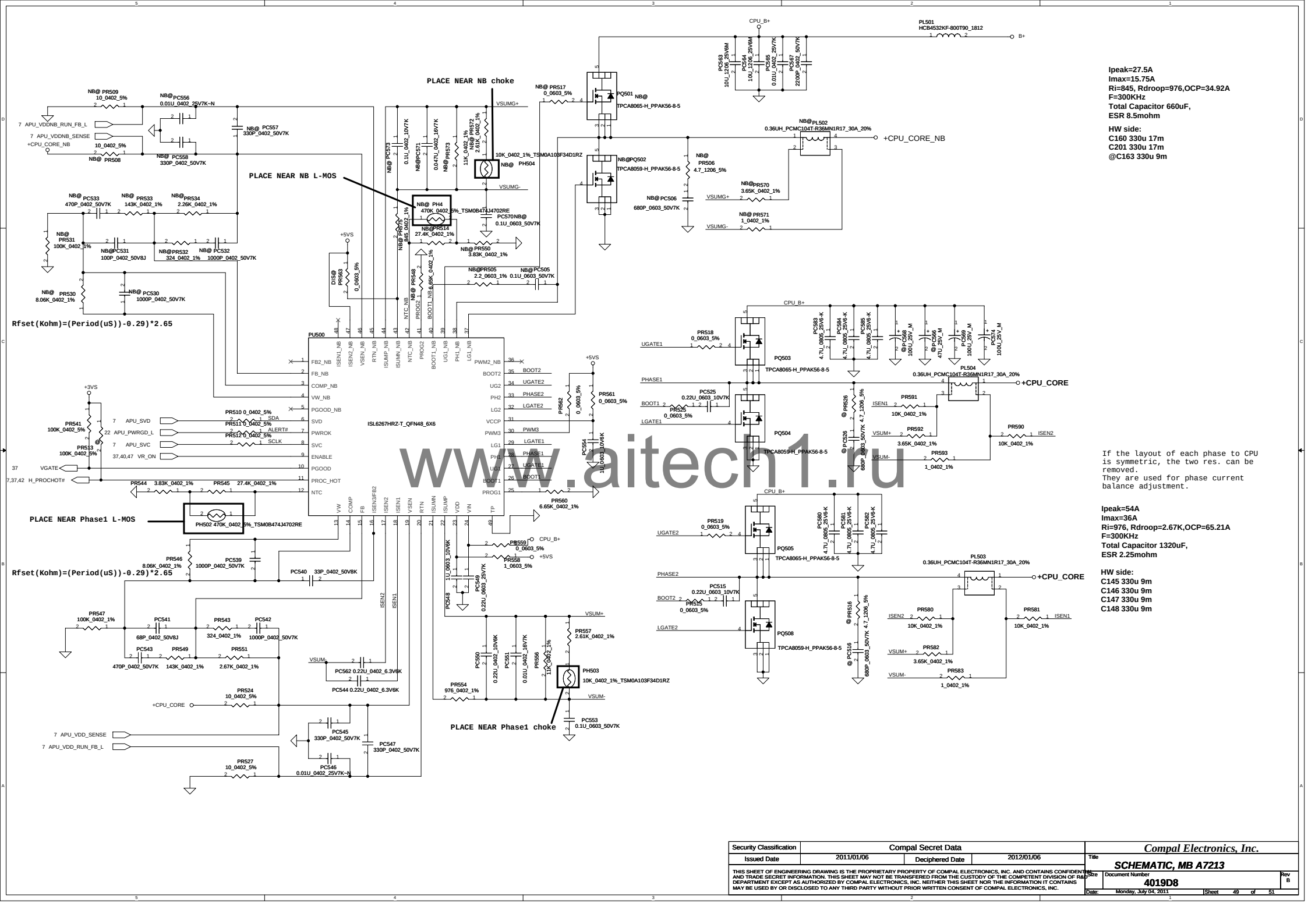


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| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|
| | 2011/03/30 | 42 | Change PR22 to 180Ω,PR28 to 1.18KΩ | For 65W SKU |
| | | | Change PR22 to 523Ω,PR28 to 3KΩ | For 90W SKU |
| | | 43 | Change PC217 to SE074102K80,PR236 to 200KΩ,PR237 to 47KΩ<br>PR205 to 3.3Ω,PR235 to SD00000S120,Add PR206,PC206,<br>Delete PC211 | Circuit modify |
| | | | Change PR222 to 53.6KΩ,PR223 to 20KΩ,Delate PQ209 | For 90W SKU |
| | | | Change PR222 to 75KΩ | For 65W SKU |
| | | 44 | Change PR335,PR355 to 2.2Ω,PC332,PC352 to SF000002080<br>,PL332,PL352 to SH00000KN00,Add PR336,PR356,PC336,PC356 | Circuit modify |
| | | 45 | Change PR155 to 2.2Ω,PC152 to SF000002080,<br>Add PR156,PC156,PR521,Delete PC260 | Circuit modify |
| | | | Change PR157 to 5.9KΩ,PL152 to SH00000IP00 | For 90W SKU |
| | | | Change PR157 to 14KΩ,PL152 to SH00000CN00 | For 65W SKU |
| | | 46 | Change PR405 to 2.2Ω,PC402 to SF000002080,Add PR406,PC406<br>Change PR407 to 14KΩ,PL402 to 2.2UH 7*7 | Circuit modify |
| | | 47 | Change PR455 to 2.2Ω,PR457 to 18KΩ,PL452 to 2.2UH 7*7<br>Add PR456,PC456 | Circuit modify |
| | | 48 | Change PR624 to 165KΩ,PR631 to 100Ω,Delete PR630,<br>Add PC636,PR520 | Circuit modify |
| | | 49 | Change PR505 to 2.2Ω,PR560 to 6.65KΩ,PR551 to 2.67KΩ<br>Change PH503,PH504 to SL200000W00,PC569,PC574 to SF000003W00<br>Add PC506,PR506,PR517,PR518,PR519 | Circuit modify |

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# HW PIR (Product Improve Record)

QHRAE LA-7213P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

| Item | Date | Page | Solution | Request |
|---|---|---|---|---|
| 1. | 3/17 | P23 | Remove level-shifter for ODD_PLUGIN# | ODD has internal 1K pull-down |
| 2. | 3/17 | P34 | Add level-shifter for CR_CPPE# | For leakage issue |
| 3. | 3/17 | P23 | Change HDMI_HPD to GEVENT10# and reserve GEVENT19# | GEVENT9# has issue |
| 4. | 3/17 | P24 | Change LOGO_LED to GPIO176 and WL_BT_LED to GPIO177 | For LED flash issue after power-on |
| 5. | 3/24 | P10 | Add C295,C316,C324,C325 | For EMI test |
| 6. | 3/28 | P39 | Reserve C20,C21,C229,C231~C236,C247,C251 | For ESD test) |
| 7. | 3/29 | P38 | Change LPC debug port to 16pins connector | To support new debug card |
| 8. | 3/30 | P07 | Add R70,R102,R105 | Pull-down for unused HPD port |

REVISION CHANGE: 0.2 TO 1.0

| Item | Date | Page | Solution | Request |
|---|---|---|---|---|
| 1. | 4/15 | P31 | Reserve D24, D25 | |
| 2. | 4/27 | P22 | Change R257 form 100k to 10k for leakage issue. | |
| 3. | 4/27 | P37 | Add BACO_EN# to EC | To inform EC GPU thermal sensor status |

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